Solid-State Electronics 53 (2009) 865–868

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# Si and SiGe faceting during selective epitaxy

Clément Pribat *, Germain Servanton, Linda Depoyan, Didier Dutartre

*STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France*

ARTICLE INFO

*Article history:*
Received 1 March 2009
Received in revised form 28 April 2009
Accepted 29 April 2009
Available online 17 June 2009

The review of this paper was arranged by Prof. A. Zaslavsky

*Keywords:*
Silicon
Silicon–germanium
Faceting
Selective epitaxy
Twin

ABSTRACT

Facet apparition during selective epitaxial growth of silicon and silicon–germanium alloys is reported in terms of morphology and kinetics. Epitaxial growth was performed on (0 0 1) Si wafers by chemical vapour deposition using the $H_2/HCl/SiH_2Cl_2$ chemistry for silicon and $GeH_4$ addition for silicon–germanium alloy. The (0 0 1) Si and SiGe growth rate was found to be limited by chlorine desorption at low temperature. The creation and development of (3 1 1) facets has been clearly explained by the epitaxial growth kinetics considerations. The impact of the deposition conditions, of the pattern structure and also of the dielectric nature on faceting are discussed here and analysed, thanks to cross section scanning electron microscopy (XSEM) and cross section transmission electron microscopy (XTEM) observations.
© 2009 Elsevier Ltd. All rights reserved.

## 1. Introduction

Faceting is a fundamental concern in crystal growth. It is observed either when the system is allowed to minimize its free energy (thermodynamic equilibrium) [1–3] or when the growth of certain crystal orientations is constrained by adsorbed molecules or atoms (kinetics limitations, the usual situation when chemical vapour deposition is concerned) [4–6]. Compared to the equilibrium shape of crystals, growth faceting depends on material properties but also on sample configurations and process conditions (pressure, temperature, chemistry, etc.).

Nowadays, the origin of this phenomenon is still the object of many controversies. However, in silicon technology, the increase of integration requires a better understanding and control of this phenomenon. Therefore, faceting can either be favoured and used in order to improve electrical performance as in folded devices [7], or minimized and suppressed as in silicon on nothing (SON) technology. Fig. 1 is an example of faceting at the SiGe/Si selective epitaxial growth (SEG) step, during a standard SON process [8]. Faceting during SEG leads to locally non-uniform films or area loss. In the structure of Fig. 1, the SEG stack is turned into a localized silicon on insulator (SOI) structure by selective etching of the sacrificial SiGe layer followed by deposition of a dielectric material in the so-formed cavity. The SiGe SEG faceting makes the access for selective etching more difficult and the Si SEG faceting will produce a non-uniform SOI film. Therefore, faceting has become a significant and critical characteristic of the epitaxial layer in this type of applications.

In the present contribution, faceting during silicon and SiGe SEG is investigated as a function of process conditions, surface configuration, pattern material and sample structure. The results are then discussed, in order to determine the root causes of this phenomenon. Consequently, our conclusions should be usable for faceting predictions in various configurations.

## 2. Experimental details

Our studies of Si (respectively $Si_{0.75}Ge_{0.25}$) faceting is based on Si ($Si_{0.75}Ge_{0.25}$) SEG realized by rapid thermal chemical vapour deposition (RTCVD) in an industrial single wafer reactor (200 mm) CENTURA (Applied-Materials). The Si ($Si_{0.75}Ge_{0.25}$) SEG were realized on (0 0 1) silicon surface orientation at various temperatures. Two kinds of substrates were fabricated with similar ⟨1 1 0⟩-aligned patterns (22% opening) but with different hard masks: one with a 7 nm-thick thermal oxide ($SiO_2$) and the other with a 20 nm-thick silicon nitride layer ($Si_3N_4$) deposited on a 20 nm-thick oxide (TEOS). The global structure is constituted by alternating thick (50–60 nm) films of Si ($Si_{0.75}Ge_{0.25}$) and thin (5–10 nm) films of $Si_{0.9}Ge_{0.1}$ (Si). The thin films constitute markers that highlight facet propagation during SEG and allow kinetics measurement. The thickness, and eventually the Ge content, of markers have been minimized in order to reduce their possible influence on growth. For both types of wafers ($SiO_2$ and $Si_3N_4$ hard

* Corresponding author. Tel.: +33 4769 25911.
*E-mail address:* clement.pribat@st.com (C. Pribat).

0038-1101/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2009.04.038

masks) and for a given material (Si or SiGe), a strictly identical process was used. The Si SEG were obtained using the $H_2$/HCl/$SiH_2Cl_2$ chemistry between 750 °C and 850 °C, whereas the $Si_{0.75}Ge_{0.25}$ ones were obtained by $GeH_4$ addition, between 650 °C and 750 °C. In this latter case, the $GeH_4$ flow has been adjusted to compensate for the Ge content variation with temperature in order to keep a fixed Ge content in the $Si_{0.75}Ge_{0.25}$ alloy.

## 3. Results

### 3.1. Morphology

Fig. 2 shows the morphology of Si SEG, realized on a nitride mask, as a function of deposition temperature. At 850 °C (high temperature, HT), and for a deposition thickness of about 300 nm, a (3 1 1) facet is clearly observable. It extends on more than 400 nm with a nearly perfect morphology. Small (1 1 1) and (−1 1 1) facets (respectively, from the top to the bottom) join the (3 1 1) facet to the dielectric at the edge of the selective epitaxial deposit. On the contrary, at 750 °C (low temperature, LT), such a (3 1 1) facet is not visible and in addition, the morphology together with the crystalline quality, as checked by TEM (not shown here), is very poor. The temperature decrease induces an important crystal quality degradation: only a few defects at 850 °C and a rather chaotic structure at 750 °C. Also note that at 750 °C the overgrowth is about 400 nm as compared to 100 nm at 850 °C. This can be explained by the rough side surface, providing many adsorption sites for the gaseous molecules, thus locally enhancing the silicon growth rate.

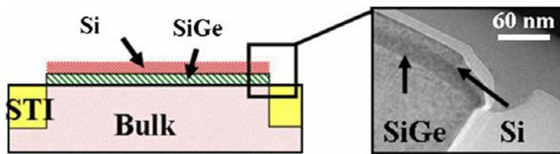


**Fig. 1.** Standard SiGe/Si SEG for the SON application. TEM picture reveals the SiGe and Si faceting at the edge of the stack.

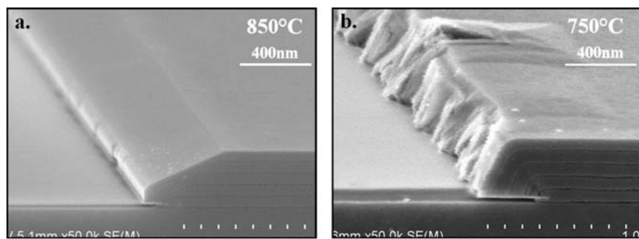


**Fig. 2.** Tilted views of two Si SEG realized on nitride mask at high and low temperature: (a) 850 °C and (b) 750 °C.

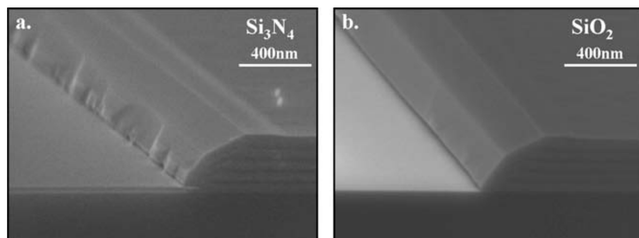


**Fig. 3.** Tilted views of two SiGe SEG realized at high temperature (750 °C) on (a) nitride and on (b) oxide masks.

Fig. 3 presents the SiGe SEG morphology at 750 °C as a function of the dielectric mask. Note that 750 °C is a rather high deposition temperature for SiGe (see the next section on kinetics). Both (3 1 1) and (1 1 1) facets are well defined and present comparable extensions in this configuration. As compared to Si (HT), the SiGe (3 1 1) facet is much smaller and the (1 1 1) facet larger. In the oxide case, the SiGe/dielectric junction consists in a (−1 1 1) plane. Note also the excellent crystalline quality of the SEG structure. On the other hand, in the case of nitride, the presence of some defects at the SEG edge makes the facet identification at the SEG/dielectric contact less easy. Moreover the growth rate conditions are less favourable for the deposition of a high quality epitaxial film.

Fig. 4 shows the Si and SiGe SEG for the 2 types of masks in the less defective temperature domain. These XSEM observations were used to determine the growth kinetics of the various planes (reported in the next figure) and to characterize the SEG/dielectric junction. On the oxide mask, the junction plane systematically consists in (−1 1 1) facets, whatever the temperature. The situation is different on nitride: junction planes are not clearly defined at high temperature (850 °C for Si and 750 °C for SiGe). As a consequence, the nature of the mask seems to play a clear role on the overgrowth faceting. For SiGe material and at 700 °C, because of the presence of defects, we can also note the change of the (1 1 1) and (3 1 1) facets into other presumably vicinal planes.

### 3.2. Growth kinetics

In the present experiments, i.e., in the range of temperatures investigated and with the $H_2$/HCl/$SiH_2Cl_2$ chemistry, silicon epitaxial growth is supposed to be mainly limited by surface reactions which require silicon precursor molecules ($SiH_2Cl_2$ at LT and $SiCl_2$ coming from $SiH_2Cl_2$ pyrolysis at HT) [9]. The silicon molecular precursors must adsorb onto the surface and react to release silicon atoms and the accompanying hydrogen and chlorine reaction

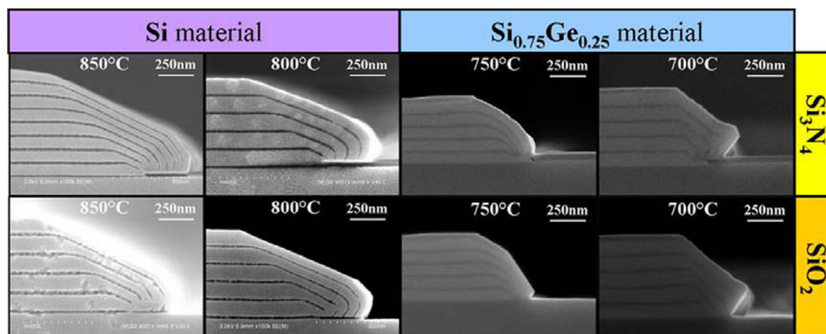


**Fig. 4.** XSEM views of Si and SiGe SEG for the two types of mask in the less defective temperature domain. Top images correspond to nitride mask and bottom images correspond to oxide mask. For the Si material a chemical revelation is necessary to differentiate the markers from the films whereas the image contrast is fine for SiGe.

Download English Version:

https://daneshyari.com/en/article/748741

Download Persian Version:

https://daneshyari.com/article/748741

Daneshyari.com