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Exact extraction method of trap densities at insulator interfaces using quasi-static capacitance–voltage characteristics and numerical solutions of physical equations

Mutsumi Kimura [a,b,c,*], Takashi Kojiri [d], Akihiro Tanabe [d], Takeyoshi Kato [e]

[a] Department of Electronics and Informatics, Ryukoku University, Otsu 520-2194, Japan
[b] Joint Research Center for Science and Technology, Ryukoku University, Seta, Otsu 520-2194, Japan
[c] Innovative Materials and Processing Research Center, High-Tech Research Center, Seta, Otsu 520-2194, Japan
[d] Research and Development Center, Zeon Corporation, Kawasaki, Kawasaki 210-9507, Japan
[e] Electronics Materials Division, Zeon Corporation, Chiyoda, Tokyo 100-8246, Japan

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ABSTRACT

An exact extraction method of trap densities at insulator interfaces (D_{it}) has been developed using quasi-static capacitance–voltage (*C*–*V*) characteristics and numerical solutions of physical equations. First, the surface potential (ϕ_s) is calculated from the *C*–*V* characteristic by applying $Q = CV$ to the insulator. Next, the flat-band voltage (V_{fb}) is determined by utilizing the fact that the total change of ϕ_s is equal to the bandgap energy (E_g). Subsequently, the electric potential (ϕ), electron density (n), and hole density (p) are calculated in the entire semiconductor by numerically solving the Poisson equation and carrier density equations so that the calculated surface potential (ϕ_s') is equal to the measured ϕ_s. Finally, D_{it} is extracted by applying Gauss's law to the insulator interface. D_{it} at an interface between a SiN_x film deposited at low temperature and a Si wafer is extracted as an example.

1. Introduction

Trap densities at interfaces between insulators and semiconductors (D_{it}) are some of the main determinants of transistor performances [1]. Recently, insulators deposited at low temperature are being developed especially for thin-film transistors (TFTs) [2,3]. Such insulators often form many D_{it} with unexpected energy distributions. Therefore, it is important to extract D_{it} in order to improve transistor performances, diagnose fabrication processes, etc.

Conventionally, there are several extraction methods of D_{it}. Charge pumping methods [4], subthreshold swing methods [1], and trans-conductance methods [5] are frequently used. However, it is necessary in these methods to fabricate metal-insulator-semiconductor field-effect transistors (MISFETs). Conventional quasi-static capacitance–voltage (*C*–*V*) methods [6] are also commonly used, in which it is merely necessary to fabricate MIS diodes. However, it is necessary to evaluate the differences between the measured capacitances and ideal capacitances of the MIS diodes without D_{it}. One method to decide the ideal capacitances is a depletion-layer approximation, but the depletion-layer approximation includes unacceptable errors especially where the free carriers gradually change, which occurs when D_{it} near the midgap is extracted. Another method is a high-frequency *C*–*V* measurement, which has been successfully used, but the high-frequency *C*–*V* measurement is subject to several undesirable effects dependent on the measurement frequency, for example, traps that capture and release carriers slower than the measurement frequency cannot be extracted.

In this study, an exact extraction method of D_{it} has been developed using quasi-static *C*–*V* characteristics and numerical solutions of physical equations. Although traps slower than the measurement frequency cannot be extracted, fairly slow traps can be extracted in comparison with the high-frequency *C*–*V* measurement. First, the surface potential (ϕ_s) is calculated from the *C*–*V* characteristic by applying $Q = CV$ to the insulator. Next, the flat-band voltage (V_{fb}) is determined by utilizing the fact that the total change of ϕ_s is equal to the bandgap energy (E_g). Subsequently, the electric potential (ϕ), electron density (n), and hole density (p) are calculated in

* Corresponding author at: Department of Electronics and Informatics, Ryukoku University, Otsu 520-2194, Japan. Tel.: +81 77 543 5111; fax: +81 77 543 7794.
E-mail addresses: mutsu@rins.ryukoku.ac.jp, mutsu@mx2.canvas.ne.jp (M. Kimura).

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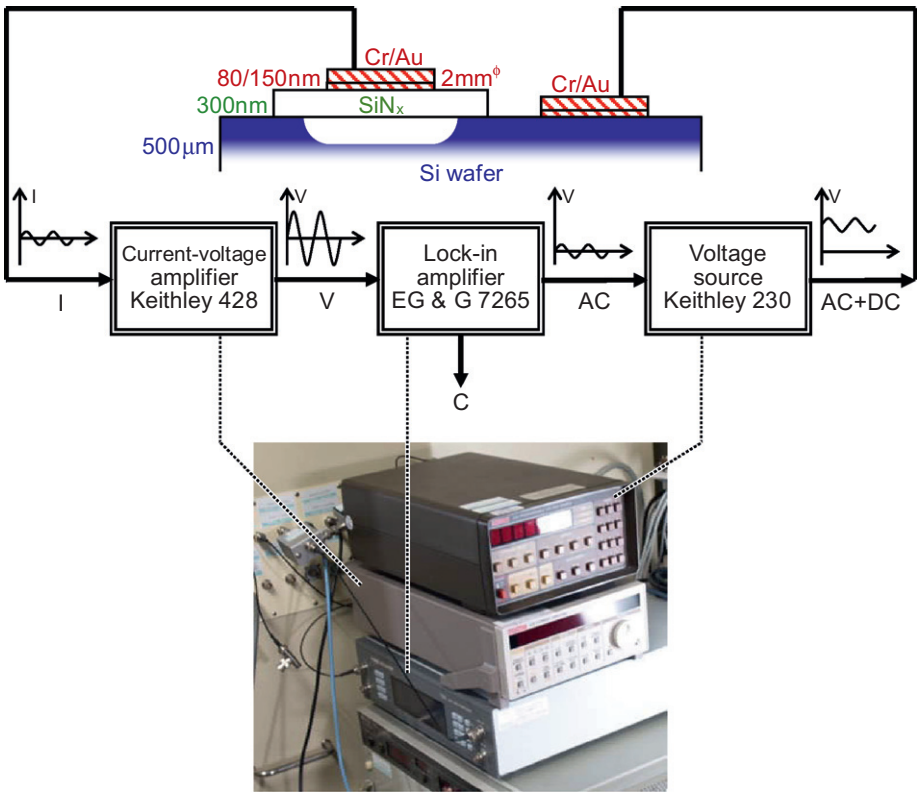

Fig. 1. MIS diode sample and measurement system.

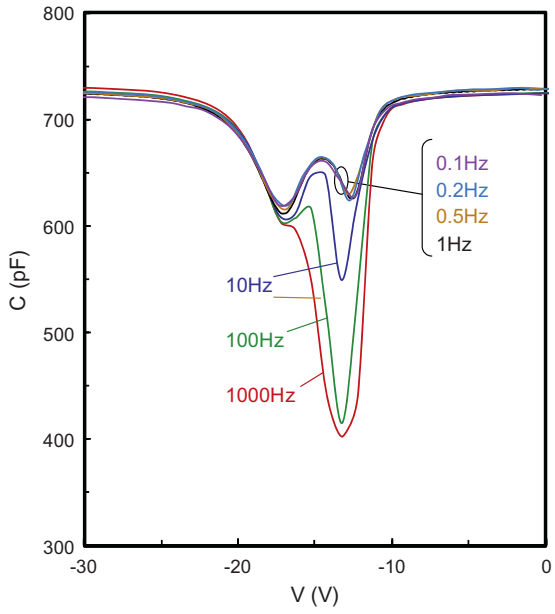

Fig. 2. *C–V* characteristics as a function of *f*.

the entire semiconductor by numerically solving the Poisson equation and carrier density equations so that the calculated surface potential (ϕ_s') is equal to the measured ϕ_s. The algorithm for numerically solving them is a novel point in this study, which is minutely described particularly in this paper. Finally, D_{it} is extracted by applying Gauss's law to the insulator interface. D_{it} at an interface between a SiN_x film deposited at low temperature and a Si wafer is extracted as an example.

2. Sample fabrication and characteristic measurement

The MIS diode sample is fabricated as an example. Fig. 1 shows the MIS diode sample. First, a Si wafer is used as a substrate, whose thickness is 500 μm, dopants are p-type boron (B), resistivity is 3 Ωcm, and then dopant density is 4.3×10^{15} cm^{-3} [7]. Next, a SiN_x film is deposited as an insulator using chemical vapor deposition (CVD) of SiH_4 and NH_3 at 300 °C, whose thickness is 300 nm. Subsequently, Cr and Au films are deposited as electrodes using vacuum evaporation through a physical mask, whose thicknesses are 80 and 150 nm and pattern diameter is 2 mm.

The *C–V* characteristics are measured as follows. Fig. 1 also shows the measurement system [8]. A lock-in amplifier, EG & G 7265, generates a small AC voltage, a voltage source, Keithley 230, superimposes a DC offset voltage, and it is applied to the Si wafer. A current-voltage amplifier, Keithley 428, amplifies a charging and discharging current through an electrode on a SiN_x film and converts it to a voltage signal, and it is returned to the lock-in amplifier. The lock-in amplifier calculates and outputs a capacitance component and conductance component from the amplitude and the phase shift of the voltage signal. It should be noted that the voltage is applied to the Si wafer and the current is measured from the electrode on the SiN_x film. Since the electrode on the SiN_x film is much smaller than the Si wafer, random noises from peripheral environments can be reduced in comparison with the opposite case. As a result, the sign of the DC offset voltage must be reversed, because the voltage is usually applied to electrodes on insulators.

The measurement frequency (*f*) must be extremely low to get quasi-static *C–V* characteristics, where the spatial distributions of ϕ, *n*, and *p* in the semiconductors are uniform and the trapping ratio of D_{it} is saturated. Fig. 2 shows the *C–V* characteristics as a function of *f*. In this example, it is found that whereas the *C–V* characteristic changes as *f* decreases from 1000 Hz to 1 Hz, it does not change even when *f* decreases below 1 Hz. Therefore, the