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Inverter circuits on glass substrates based on ZnO-nanoparticle thin-film transistors

K. Wolff *, U. Hilleringmann

University of Paderborn, Institute of Electrical Engineering and Information Technology, 33095 Paderborn, Germany

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ABSTRACT

The integration technique and the properties of inverter circuits on glass substrates using ZnO nanoparticles as semiconductor material are presented. The inverter device consists of a switching and a load metal–insulator–semiconductor field-effect transistor with poly(4-vinylphenol) as the gate dielectric. Although the semiconductor is deposited by spin-coating of a colloidal ZnO dispersion and the process temperature is limited to 200 °C, the inverters show reasonable maximum peak gains at low power consumption. The maximum peak gain was 6 V/V, whereas the maximum static power dissipation density was less than 26 nW/μm^2. Additionally, the influence of the geometry ratio as well as of the supply voltage on the device performance has been investigated. With regard to the optical characteristics, the proposed technique leads to circuits with an optical transmittance of up to 80%.

1. Introduction

Metal oxide semiconductors have received much attention for low-cost electronic applications [1,2], partly because of the degradation difficulties in organic devices. In particular, zinc oxide is a promising candidate for flexible, transparent and printable thin-film transistors (TFT), while it is commonly deposited as a nanostructured material like nanorods, nanowires or nanoparticles [2,3], or by sol–gel method [4], whereas either the nanomaterial or the precursors are spin-coated on the surface. Even TFTs integrated by inkjet-printing technique have been demonstrated [5]. However, solution-processing via the sol–gel route is in need of relatively high temperatures for the precursor decomposition [6,7]. Although there are reports of nanomaterial-based transistor devices, which show reasonable characteristics, logic circuits are usually integrated via sputtering, atomic layer deposition or pulsed laser deposition (PLD) techniques of ZnO or related materials like zinc tin oxide or indium gallium zinc oxide [8–11]. However, if nanoparticles are used as a semiconductor layer, either the performance is in need of improvement or the required thermal budget is too high for glass or even plastic substrates.

After nanoparticle-based inverter circuits on silicon substrates have been demonstrated in [12], this paper deals with inverters on glass substrates, which are based on bottom-gated Schottky-barrier Drain/Source TFT. Due to the optical transparency of the substrate, the semiconductor and the gate dielectric layer, the entire device is transparent in the optical wavelength spectrum.

In order to demonstrate a low-cost integration route, all processes are kept as simple as possible, e.g. ZnO is deposited by spin-coating of a commercial, aqueous colloidal suspension and *poly(4-vinylphenol)* (PVP) is used as gate dielectric layer [12,13]. Furthermore, all temperatures during the integration process are below or equal to 200 °C.

2. Device integration

The inverters were integrated on borosilicate glass substrates (Plan Optik AG, Germany), which were cleaned prior to integration by Caro's etch solution (H_2SO_4/H_2O_2) and subsequent rinsing in DI water. First, a thin Al-layer (30 nm) was electron beam evaporated and structured to form the gate-electrodes.

Next, a *poly(4-vinylphenol)* (PVP) gate-dielectric was deposited from a PVP solution by spin-coating. Contact vias to the gate-electrodes were etched using a reactive ion etching system with oxygen plasma. The PVP solution composition, the deposition parameters as well as the etching parameters are reported in [12]. The AFM topography reveals a PVP layer thickness of 180 nm, while the root mean square roughness of the PVP layer is 5.7 nm.

Then, a layer of ZnO nanoparticles was deposited from an aqueous dispersion, which had been received from EVONIK DEGUSSA GMBH, Germany. According to SEM analysis, a spin-coating deposition at

* Corresponding author. Address: University of Paderborn, EIM-E/Sensor Technology Group, Warburger Strasse 100, 33098 Paderborn, Germany. Tel.: +49 5251 605908; fax: +49 5251 605913.

E-mail addresses: wolff@sensorik.upb.de (K. Wolff), uhill@mail.upb.de (U. Hilleringmann).

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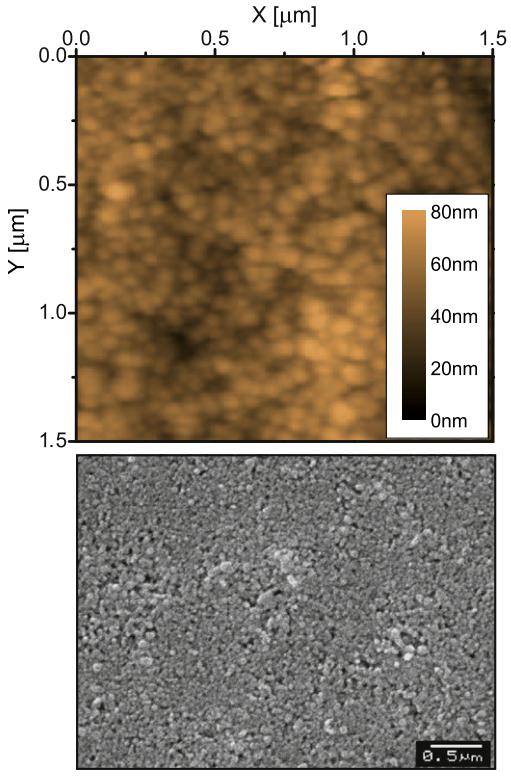

Fig. 1. Non-contact mode AFM topography (top) and SEM micrograph (bottom) of the ZnO nanoparticle layer (top view) after the annealing for 1 h at 200 °C.

2000 rpm and a subsequent soft-bake process at 110 °C for 300 s resulted in films with a thickness of 250–300 nm. To cause a minimal sintering of the nanoparticles, the samples were once again annealed for 1 h at 200 °C in ambient atmosphere. However, the layer thickness was not affected by the annealing process. The layer quality was monitored by atomic force microscopy (AFM) and scanning electron microscopy (SEM). Both methods confirm that the effective particle size of approximately 100 nm is unchanged in comparison to the as-dispersed nanoparticles in the suspension (Fig. 1). Therefore, the semiconductor layer is characterized by nanocrystallinity with domain sizes of the effective particle diameter. Primary particles are not supposed to be visible, because they are not isolated in the dispersion [14]. A few pinholes are visible in the SEM micrograph in Fig. 1, but since their areal density is sufficiently low, they are not opposed to device integration. A root mean square roughness of 11.8 nm was determined from the AFM topography of the annealed ZnO film. Finally, the deposition and structuring of the metal interconnects and drain-/source-electrodes by a gentle lift-off technique of an e-beam evaporated aluminum layer (200 nm) completed the device integration.

3. Results and discussion

On-wafer electrical measurements at room temperature in darkness were performed using a HP 4156A Precision Parameter Analyzer. The relative humidity was approximately 40% throughout all measurements.

3.1. Individual transistor devices

The integrated individual transistor showed reasonable electrical characteristics, whereas a hysteresis in the transfer characteristics was observed. The hysteresis, which causes a threshold voltage

Table 1
Typical properties of individual transistors used for inverter integration. All values are given for V_{DS} = 5 V.

Parameter	Value
Field-effect mobility μ_{FE}	0.08 cm^2 (V s)$^{-1}$
Threshold voltage[a] V_{tf}	5.9 V
Threshold voltage[b] V_{tb}	1.9 V
I_{ON}/I_{OFF}	~10^6
Subthreshold slope *SS*	1.74 V/dec

[a] Forward sweep (V_{tf} = −4.4 V @ V_{DS} = 20 V).
[b] Backward sweep (V_{tb} = −11.1 V @ V_{DS} = 20 V).

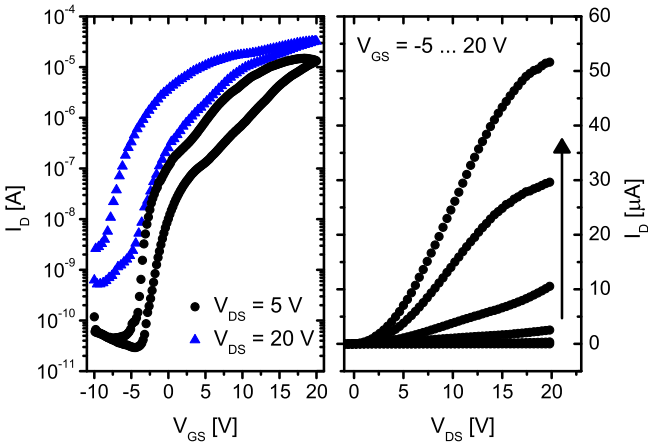

Fig. 2. Transfer and output characteristics of a typical ZnO nanoparticle FET (L = 3 µm, W = 500 µm). The transfer characteristics are plotted for V_{DS} = 5 V (black circles) and V_{DS} = 20 V (blue triangles). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

shift, is attributed to charge trapping in the PVP gate-dielectric [15]. Since OH^- radicals in the PVP are known to trap free charges, the hysteresis indicates an incomplete cross-linking [16]. Furthermore, the ZnO nanoparticle TFT exhibited a severe dependency on V_{DS} leading to altering transistor modes during operation [17]. The transistor parameters are shown in Table 1, while typical characteristics are plotted in Fig. 2. Note that the threshold voltages for V_{DS} = 5 V are positive, while they are negative for V_{DS} = 20 V. The transistor parameters were extracted using the linear extrapolation method in the saturation regime (linear extrapolation of the $\sqrt{I_D} - V_{GS}$-curve) for the threshold voltage and the field-effect mobility for the charge carrier mobility. Both methods are common and well-established for the parameter extraction of devices with potentially non-ideal electrical contacts as well as known for their reproducibility [18]. Nevertheless, it has to be mentioned that the linear extrapolation method for derivation of the threshold voltage is sensitive to series resistance and mobility degradation [19]. As can be seen from the output characteristics, the series resistance becomes less dominant in the saturation regime and the calculated value can be assumed to be correct. The contact properties also affect the field-effect mobility, which is, however, characteristic for this method.

The reproducibility of the device properties is an important issue for inverter fabrication. Since the threshold voltage is of particular interest for logic circuit integration, the V_{th} distribution is depicted in Fig. 3. As observed before, the threshold voltage is dependent on the sweep direction. The mean values for the forward and backward sweep are $\overline{V_{tf}} = 0.4$ V and $\overline{V_{tb}} = -2.3$ V, respectively. Remarkably, the standard deviation of V_{th} for both sweep direction is 1.55 V. With regard to the current early state of the inverter integration, the widely spread threshold voltages are tolerable. However, improvement of reproducibility has to be addressed within future work.