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Influence of processing and annealing steps on electrical properties of InAlN/GaN high electron mobility transistor with Al_2O_3 gate insulation and passivation

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ABSTRACT

We report on preparation and electrical characterization of InAlN/AlN/GaN metal–oxide–semiconductor high electron mobility transistors (MOS HEMTs) with Al_2O_3 gate insulation and surface passivation. About 12 nm thin high-κ dielectric film was deposited by MOCVD. Before and after the dielectric deposition, the samples were treated by different processing steps. We monitored and analyzed the steps by sequential device testing. It was found that both intentional (ex situ) and unintentional (in situ before Al_2O_3 growth) InAlN surface oxidation increases the channel sheet resistance and causes a current collapse. Post deposition annealing decreases the sheet resistance of the MOS HEMT devices and effectively suppresses the current collapse. Transistors dimensions were source-to-drain distance 8 μm and gate width 2 μm. A maximum transconductance of 110 mS/mm, a drain current of ~0.6 A/mm (V_{GS} = 1 V) and a gate leakage current reduction from 4 to 6 orders of magnitude compared to Schottky barrier (SB) HEMTs was achieved for MOS HEMT with 1 h annealing at 700 °C in forming gas ambient. Moreover, InAlN/GaN MOS HEMTs with deposited Al_2O_3 dielectric film were found highly thermally stable by resisting 5 h 700 °C annealing.

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1. Introduction

In last several years, InAlN/GaN based high electron mobility transistors (HEMTs) have been intensively studied as candidates for next generation high-power and high frequency devices [1]. The main advantage of InAlN/GaN heterostructure compared with commercially available AlGaN/GaN HEMTs is that the InAlN thin film can be grown lattice matched on the GaN buffer layer offering high charge density in the channel, high thermal and chemical stability [1,2]. However, HEMTs degradation may appear due to a high gate leakage current of these devices [3]. Thus, the introduction of gate insulation promises to be an efficient approach to overcome this drawback. In previous works, a number of gate dielectrics such as ZrO_2 [4], HfO_2 [4] or Al_2O_3 [5–8] have been used in metal–oxide–semiconductor (MOS) InAlN/GaN HEMTs to reduce the gate leakage current. However, most serious issues arise from the InAlN surface- or the dielectric/InAlN interface-related

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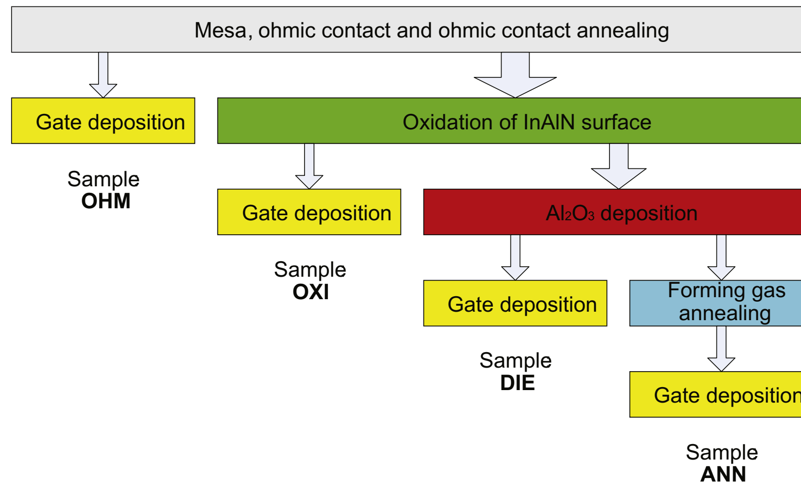

Fig. 1. Process scheme.

imperfections that can lead to the drain current collapse (gate-lag). Gate-lag represents reduction of the output drain current in pulse regime compared to that of DC regime and limits HEMTs RF and switching performance. This effect has been explained by the filling and emptying of relatively slow interface states [9,10]. Thus performance of GaN-based MOS HEMTs strongly depends on the quality of the gate dielectric/InAlN interface. Therefore, in addition to a high insulating capability, the gate dielectric should also passivate deep levels on the InAlN surface. However, dielectrics based on oxides are prepared in oxygen assisted atmosphere. It was reported elsewhere that oxygen may generate deep level states on the surface of GaN based materials [11–13]. Alternatively, one may avoid usage of oxides by using SiN films [14,15] but in this case a relatively low band gap (5.3 eV) as well as low dielectric constant ($\kappa \sim 7$) of SiN dielectrics may not be sufficient for GaN-based devices.

In this work, we prepared InAlN/AlN/GaN MOS HEMT structures with Al_2O_3 gate dielectric deposited by MOCVD for the gate insulation and surface passivation. We study the role of each processing step in the MOS device preparation chain in detail, such as surface oxidation, dipping in HCl or post-deposition annealing.

2. Experimental details

$In_{0.18}Al_{0.82}N$/GaN heterostructure was grown by MOCVD on sapphire substrate. As reported elsewhere, interface roughness and alloy disorder may dominate the scattering mechanisms in InAlN/GaN [16]. Therefore, 1 nm-thick AlN spacer was applied between InAlN (13 nm) and GaN to reduce the alloy disorder scattering [17]. Two-dimensional electron gas (2DEG) carrier density was found to be 1.6×10^{13} cm^{-2} and carrier mobility was found to be 1182 cm^2 V^{-1} s^{-1}. An ohmic Ti(30 nm)/Al(150 nm)/Ni(40 nm)/Au(50 nm) metallization was annealed at 800 °C for 120 s.

We study the role of each processing step of the MOS device preparation chain in a detail. The substrate has been divided into five parts with marks: OHM, OXI, DIE, ANN and LONG_ANN. These marks also correspond to the last processing step of each sample before deposition of gate metallization. Sheet resistance was determined on each sample after each processing step on identical TLM structures. The process scheme with used marks is shown on Fig. 1.

Processing step OHM defines deposition of ohmic contacts and their annealing. The sample with mark OHM has not been passivated.

In processing step with OXI mark, samples were thermally oxidized after ohmic contacts processing. InAlN surface was ex situ oxidized at 650 °C for 2 min in O_2 atmosphere. With ex situ oxidation we wanted to stabilize InAlN surface and simulate oxidation during Al_2O_3 dielectric deposition, thus dividing deposition of dielectric film effectively into two steps. Alomari et al. presented thermal oxidation of InAlN as self-limiting process [18]. Therefore, we suppose InAlN surface will no longer be oxidized during Al_2O_3 deposition.

During DIE processing step dielectric film is deposited on oxidized InAlN surface. Prior to dielectric deposition, samples were dipped into HCl/H_2O (1:2) solution for 1 min. The 12 nm-thick Al_2O_3 dielectric film was deposited in a low-pressure hot-wall quartz MOCVD reactor. Precursor dissolved in a solvent (toluene) was introduced to the evaporation chamber using TriJet™ liquid precursor delivery technique. Deposition chamber of the MOCVD reactor was heated up to 600 °C. Aluminum acetylacetonate was used as a precursor.

Samples with marks ANN and LONG_ANN were subjected to annealing after Al_2O_3 deposition. Samples were exposed for 1 h (ANN) or 5 h (LONG_ANN) annealing at 700 °C in forming gas (N_2 was 90% and H_2 was 10%).

All samples were finalized with gate electrodes (Ni(25 nm)/Au(100 nm)) deposited using E-beam evaporation technique.

HEMT structures were processed with a gate length of 2 μm and an 8 μm drain-source opening. Circular MOS capacitors with a diameter of 100 μm were also processed. For the gate-lag experiment we used Keithley 4200 SCS with load resistor 50 Ω. The gate–source voltage was pulsed from a value below the threshold voltage (V_{th}) to V_{GS} with pulse duration 100 ns, the drain–source voltage (V_{DS}) was DC biased. The measured pulsed output characteristics were compared with DC mode output characteristics. InAlN/GaN channel sheet resistance was measured by the transfer length method (TLM) [19]. Standard DC output, input, and transfer characteristics were measured on HEMTs.

3. Results and discussion

Two-dimensional electron gas (2DEG) channel sheet resistances (R_{SH}) were measured using TLM method [19]. Sheet resistance of the as-grown InAlN/GaN structure was 330 Ω/□. Sheet resistance was measured after each processing step starting from the reference value R_{SH0} after the ohmic contact annealing towards the post-deposition annealing steps. Contact resistance of ohmic

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