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BSIM-CG: A compact model of cylindrical/surround gate MOSFET for circuit simulations

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ABSTRACT

A turnkey, production circuit simulation ready compact model for cylindrical/surround gate transistors has been developed. The core of the model contains an enhanced surface potential based description of the charge in the channel. Analytical expressions for channel current and terminal charges have been derived. A method to account for quantum confinement in the cylindrical structure in a compact model framework is described. For the first time we present calibration results of such a model to a cylindrical gate technology that also exhibits asymmetric *I–V* characteristics.

1. Introduction

The relentless scaling of the CMOS devices for purposes of performance, power and cost has led to the scouting for 3-D device structures moving away from the traditional 2-D planar MOSFET structures. The cylindrical gate structure has gained popularity with both academia and industrial research as it promises the greatest scaling potential in terms of channel length given the enhanced gate control over the channel by the all-around gate. Some of the first cylindrical surround gate devices were fabricated more than two decades ago as a prospective replacement for DRAM transistors as it would have paved way for a cell occupying the least silicon area ($4F^2$ where F is the minimum feature) [1]. More recently these devices have once again come into limelight as they are viewed as a potential replacement for logic too offering better scalability and thus more functions for a given silicon real estate. Horizontal silicon nanowires [2], twin silicon nanowires [3] and vertical pillar like structures [4] have been reproducibly manufactured at various industry class fabrication facilities, Fig. 1. Whether these point towards a complete replacement of planar transistors with cylindrical transistors can be addressed separately, however it suffices to say these devices do have near term applications such as in memories where smaller footprint area equates to a larger density.

In order to push forward to evaluate the capabilities of such devices, a compact model is required for performance analysis through circuit simulations. A compact model, unlike a simple device model or a comprehensive computer simulation model used for understanding the physics of operation, needs to provide high accuracy and computational efficiency to perform multi-million transistor circuit analysis. Extensive device modeling and simulations help in better understanding of a device and form a seed for compact models [5–7]. In a recent move towards surface potential based models that are single piece infinitely differentiable as against piece-wise modeling, a number of groups have contributed towards what could possibly form the core model for a cylindrical/surround gate transistor [8–11]. Jimenez et al proposed an analytical solution for the surface potential, drain current and charge–voltage characteristics for an intrinsic long channel transistor [8,12]. This solution was reformulated into a symmetric linearization framework to incorporate directly into the PSP compact model too [11]. Liu et al. have extended the former solution to include doping in the channel and have shown the solution to agree well with device simulation results up to doping levels of $\approx 10^{18}$ cm^{-3} [10]. Though it is known that an intrinsic channel shall tend to offer higher mobility and be immune to variability due to random dopant fluctuations, some amount of body-doping is likely to be present in order to tune the threshold voltage of the device or to offer multiple threshold voltage devices

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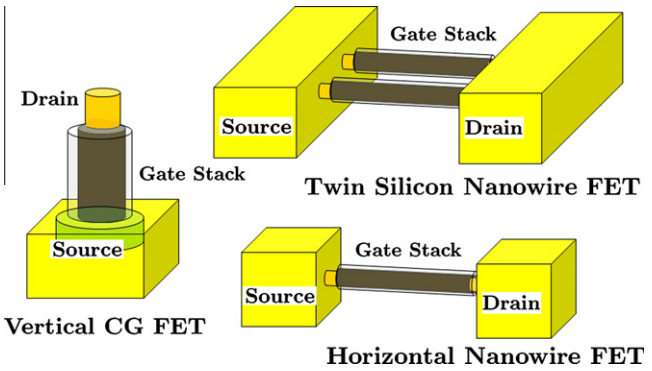

Fig. 1. Different possible structures of implementing a cylindrical gate FET on silicon.

in the same process for circuit design power-performance optimization purposes. These efforts however only address the ideal prototype device not the real device whose characteristics are determined by complex transport, short channel, leakage, and parasitic effects. The goal of this work is to culminate these efforts to a full-fledged mature compact model that could be directly used for circuit simulations.

In this work, we build many necessary details around a core model in order to create BSIM-CG. While all of them cannot be covered in a single attempt, we have chosen to demonstrate a select few interesting effects that are captured for this purpose. The surface potential equation for a doped channel is extended to include poly-depletion effects in the gate. Analytical equations for current and charge are presented. A simple yet flexible way to introduce accumulation capacitance into this framework is proposed. Quantum confinement effects that would become prominent as the diameter of these devices are scaled to below 20 nm are also modeled and included in this work. Finally we conclude by presenting some of the results obtained by fitting this model to hardware silicon data.

2. Enhanced surface potential formulation

The coordinate system that we shall use for derivations in this work is shown in Fig. 2. Symbols R, L, t_{ox}, t_{poly}, N_a, and N_{poly} represent the radius of the channel, the channel length, the gate oxide thickness, the poly-gate thickness, the channel doping and the polysilicon doping respectively.

2.1. Poly-depletion effect

The usage of metal as a gate material for CG transistors is likely as the effective oxide thickness (EOT) for sub-22 nm technology node is speculated to be $\leqslant$1 nm [13]. Using highly doped (at solubility limit) poly-silicon as a gate will still be a deterrent to achieving this EOT due to the fact that poly-depletion contributes to the increase in EOT. However for some cost constrained applications like memories it is more likely that polysilicon will still be employed as a gate material. Also for vertical device orientation scaling the length of the device is not as critical and hence EOT scaling can be relaxed. We shall model poly-depletion for cylindrical gate and incorporate it in the surface potential equation later.

The Poisson's equation in the oxide assuming no oxide charges is as follows:

$$\frac{1}{r}\cdot\frac{d}{dr}\left(r\frac{d\psi}{dr}\right)=0 \tag{1}$$

This leads to the electric field at an arbitrary point $R < r < R + t_{ox}$ in the oxide to be

$$E_{ox}(r)=E_{ox}(R)\cdot\frac{R}{r} \tag{2}$$

The voltage drop in the oxide can be derived by integrating $E_{ox}(r)$ w.r.t. r within the oxide.

$$V_{ox}=E_{ox}(R)\cdot R\cdot ln\left(1+\frac{t_{ox}}{R}\right)=E_{ox}(R)\cdot EOT \tag{3}$$

The electric field in the gate at the gate–oxide interface, E_{polyox} is given by

$$E_{polyox}=\frac{\epsilon_{ox}}{\epsilon_{gate}}\cdot E_{ox}(R+t_{ox})=\frac{\epsilon_{ox}}{\epsilon_{gate}}\cdot\frac{R}{R+t_{ox}}\cdot\frac{V_{ox}}{EOT} \tag{4}$$

where ϵ_{gate} and ϵ_{ox} are the dielectric constants of the gate and the oxide respectively.

The Poisson's equation in the gate assuming a poly-doping of N_{poly} is

$$\frac{1}{r}\cdot\frac{d}{dr}\left(\frac{d\psi}{dr}\right)=-\frac{qN_{poly}}{\epsilon_{gate}} \tag{5}$$

Integrating it once, the electric field in the poly at r, $E_{poly}(r)$ can be obtained from the below equation.

$$-E_{poly}(r)\cdot r+E_{polyox}\cdot(R+t_{ox})=\frac{qN_{poly}}{2\epsilon_{gate}}\left[r^2-(R+t_{ox})^2\right] \tag{6}$$

The electric field goes to zero at the edge of the depletion region in the polysilicon gate, i.e. at $r = R + t_{ox} + X_{dpoly}$. This gives us the value of E_{polyox} in terms of X_{dpoly} as

$$E_{polyox}\cdot(R+t_{ox})=\frac{qN_{poly}}{2\epsilon_{gate}}\left[2(R+t_{ox})+X_{dpoly}\right]X_{dpoly} \tag{7}$$

The voltage drop in the polysilicon gate, V_{poly} can now be obtained by integrating Eq. (6) w.r.t r from the gate-oxide boundary to the edge of polysilicon depletion.

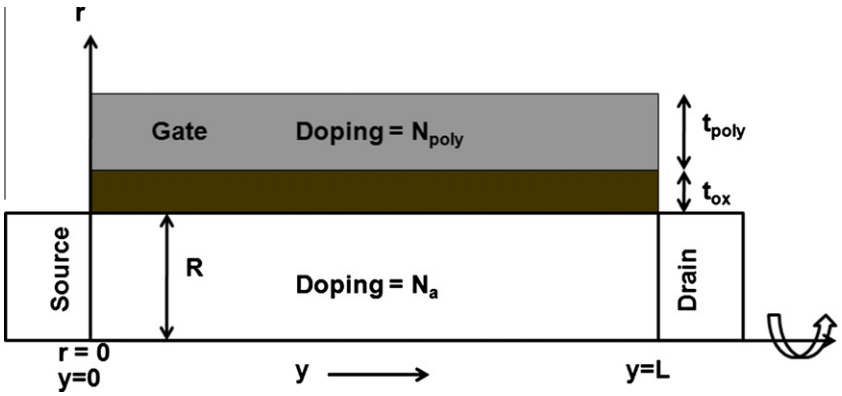

Fig. 2. Co-ordinate system convention and variables for the cylindrical gate FET.