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Abnormally high local electrical fluctuations in heavily pocket-implanted bulk long MOSFET

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ABSTRACT

For the first time, a huge drain current fluctuations degradation is shown on heavily pocket-implanted above-micrometer devices. This degradation, which is a serious concern for analog design, is attributed to the high potential barriers that stand at end sides of long devices and mainly control the device electrostatics. Because the barriers height is modulated by the gate voltage, it is demonstrated that the excess fluctuations are highly gate-bias-dependent. The classical drain current model has been shown to be inadequate to describe the current flow through the entire range of applied gate bias voltages. A new adapted model allows for a correct description of the drain current and associated fluctuations.

1. Introduction

Pocket implant technology has been developed to combat short-channel effects and enables today gate length to be in sub-50-nm regions. However, pockets or halo devices suffer from degraded analog performances. Indeed pockets are responsible for increased drain-induced-barrier-lowering and reduced output resistance for long channel devices [1,2]. These effects were attributed to additional barrier created near the drain by heavily doped pocket. Because of its drain bias induced modulation, this additional barrier creates more DIBL and less output resistance. This is a serious concern for analog design but not the only one. Indeed, there are also concerns about pocket implants impact on matching performance. Increased mismatch for short devices has been widely observed and was explained by the global increased impurities concentration in channel [3]. Since channel impurities induced mismatch is not highly concentration dependent (impurities contribution roughly increases with their concentration at the power 0.4 [4]), the increase is generally within a 20% range. However, the risk of major mismatch degradation for pocket-implanted devices that are longer than roughly twice the pocket length has not been yet reported. Unlike DIBL and output resistance performance degradation, mismatch increase that will be depicted in this paper is not directly due to the drain bias induced additional barrier lowering. Indeed matching performance is given at fixed V_d. However, the mismatch degradation is also due to this additional barrier at drain side that exists because of a non-uniform channel doping. Tanaka pointed out the key fact that is responsible for increased mismatch. Indeed he mentioned in [5] that a shrunk area controls threshold voltage. However, despite its heavy consequences for analog design, the increase was not investigated for long devices and the impact of gate voltage was not reported. In this paper, the evidence of a drastic increase of mismatch when a heavy pocket dose is used will be shown. Then it will be demonstrated that even more important than the pocket impurities concentration is the difference in impurities concentration between pocket regions and the substrate directly controls the threshold and gain factor mismatch increase for long devices. Finally the beneficial role of higher gate biasing for reducing current mismatch will be investigated.

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2. Experimental setup

2.1. Matching definition and test structures

Whereas global variations are usually due to manufacturing equipment related non-uniformities and changes over time, mismatch is the consequence of local stochastic variations that even affect closely spaced devices. Based on the definition of mismatch, the aim of matching studies is to evaluate fluctuations of electrical parameters between two identically designed devices. The matching configuration that was used for all the following experiments is made of pairs of devices with separated drain, source and gate. Considering the electrical parameter P, matching characterization consists in measuring $\Delta P = P_2 - P_1$ on each die of a wafer with P_1 and P_2 the values for devices 1 and 2, respectively. Then from such measurements, ΔP dispersion ($\sigma_{\Delta P}$) is estimated for all geometries.

2.2. Extraction methodology and data treatment

In all the experimental results presented hereafter, threshold voltage (V_t), current factor (β) and mobility attenuation factor with the gate voltage (θ_1) were extracted using Y function [6] according to (1) where V_d is the drain voltage

$$I_d = \frac{\beta \cdot V_d \cdot (V_g - V_t - V_d/2)}{1 + \theta_1 \cdot (V_g - V_t - V_d/2)} \quad (1)$$

For each geometry, $\sigma_{\Delta P}$ estimation is deduced from measured samples from which outliers are removed thanks to an iterative filter. This filter consists in successively removing the values which are out of the mean ± 3σ region and computing the mean again till there are no more samples out of this region. In this study, for each of the geometries and for all the devices, the number of tested pairs was 70 and the number of outliers varies from 0 to 3, depending on the sample. Considering this limited sample size of measured paired transistors, $\sigma_{\Delta P}$ estimation is affected by statistical dispersion. For each of the geometries, at a 99% confidence level, all the $\sigma_{\Delta P}$ results are true in a [−18%, +27%] confidence region.

3. Impact of pocket dose, substrate doping and temperature on long devices V_t fluctuations

3.1. Impact of pocket dose on V_t fluctuations

Matching measurements were performed on several sub-100-nm technological nodes devices. Four process splits from the 65 nm node were under investigation. The devices from the split called "No Pocket" are built without pocket implants whereas dose 1-2-3 splits devices are built with an increasing pocket dose (Table 1).

The V_t profiles corresponding to these four splits are shown in Fig. 1. Fig. 2 that shows normalized mismatch for every split: it is clear that whereas short devices perfectly follow scaling law – (2) and Fig. 2 – long devices strongly deviate from the law all the more as more as the pocket dose is high. Since the split without pocket does not present any deviation from the scaling law, we can conclude that the degradation is induced by pockets implants.

Table 1
Pocket implants description for the three pocket implants splits under test.

Pocket dose	Implant type	Energy (keV)	Dose (cm^{-2})
1	BF_2	50	2.50E+13
2	BF_2	50	3.00E+13
3	BF_2	50	3.50E+13

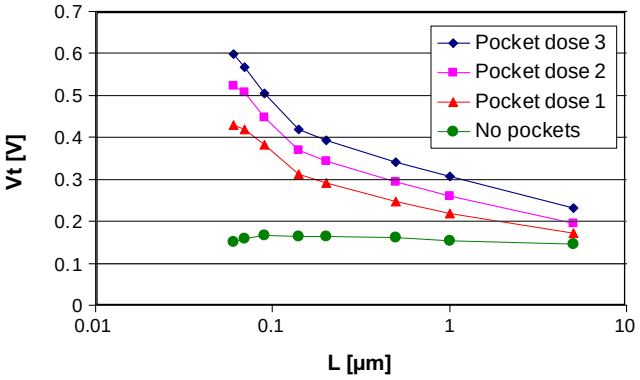

Fig. 1. V_t profile for the four implanted pocket doses NMOS.

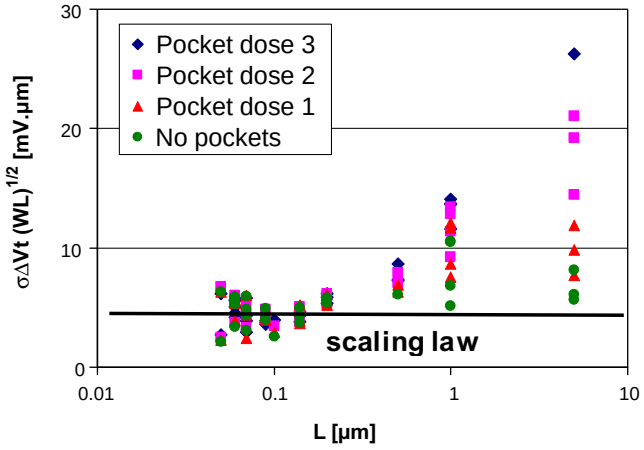

Fig. 2. NMOS threshold voltage for the four implanted pocket doses.

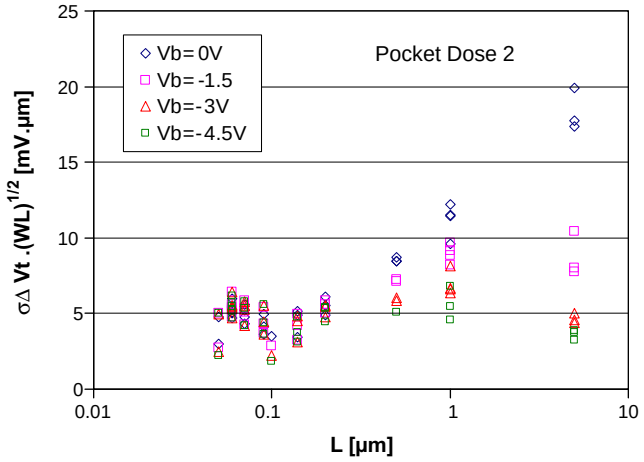

Fig. 3. V_b impact on V_t mismatch for "Pocket dose 3" NMOS.

However, it gives no clue about the physical reasons that stand behind this degradation. The idea of a global channel doping increase is dismissed since mismatch degradation would be as high as the device is short [4], which is contrary to the observations. Since it is known [7] that a heavier pocket dose can lead to more Si/SiO_2 interface traps, their random number could be the reason for this unexpected high mismatch. However the withdrawing of such degradation with strong enough bulk biasing (V_b) (Fig. 3) does