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A model for the *C–V* characteristics of the metal–ferroelectric–insulator–semiconductor structure

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ABSTRACT

A model is developed to describe the characteristics of the metal–ferroelectric–insulator–semiconductor (MFIS) structure based on the dipole switching theory (DST) and the silicon physics of metal–oxide–semiconductor (MOS) structure. The ferroelectric dipole distribution function is used to simulate the history-dependent electric field effect of the ferroelectric layer. Using the model, the thickness effects of the ferroelectric and insulator layers on the capacitance–voltage (*C–V*) characteristic and the memory window were investigated for Pt/SBT/ZrO_2/Si and Pt/BLT/MgO/Si structures. All the simulation results show good agreement with the experimental results, indicating that the model is suitable for simulating the *C–V* characteristic and the memory window of MFIS structure. In addition, the mathematical description is simple and can be easily integrated into the electronic design automation (EDA) software for circuit simulation.

1. Introduction

Ferroelectric field effect transistor (FeMFET) with a metal–ferroelectric–insulator–silicon (MFIS) structure is a promising candidate for non-volatile random access memory because of its high speed, single-device structure, low power consumption, and non-destructive read-out operation [1]. As the key part of the FeMFET, the electrical properties of the MFIS structure such as the capacitance–voltage (*C–V*) characteristic and memory window can affect the information storage capability and stability of the FeMFET [2]. Miller et al. [3–5] proposed a mathematical model in which the history-dependant effect is neglected to depict the ferroelectric polarization behavior in a metal–ferroelectric–metal (MFM) capacitor. However, this model has limitation to simulating the unsaturated polarization behaviors. Although the *C–V* characteristic and memory window of the MFIS structure have been experimentally studied widely, there are only a few theoretical studies. Based on Miller's model, Lue [6] modeled the electrical properties of the MFIS structure and the FeMFET device. In Lue's model, the simple tanh type equations were used to describe the polarization so that the history-dependent electric field effect is neglected. On the other hand, in the dipole switching theory (DST) [7], the ferroelectric dipole distribution function is usually used to depict the ferroelectric polarization behavior of the MFM capacitor in order to consider the history-dependent electric field effect. However the method has not been used for simulating the electrical properties of MFIS structure.

In this paper, we report our work on modeling the ferroelectric polarization behavior using the ferroelectric dipole distribution function in DST, in order that the history-dependent electric field effect was considered for MFIS structure. The substrate behavior was described by the silicon physics of the metal–oxide–semiconductor (MOS) structure. Using this model, the thickness effects of the ferroelectric and insulator layers on the *C–V* characteristic and memory window of MFIS structure were investigated. The parameters of the ferroelectric and insulator layers were obtained from the reported experiments of Pt/$SrBi_2Ta_2O_9$(SBT)/ZrO_2/Si and Pt/$Bi_{3.25}La_{0.75}Ti_3O_{12}$(BLT)/MgO/Si structures [8,9]. The simulation results were compared with the previous experiments, and the applicable range of the model and the dependence of *C–V* characteristic and memory window on structure parameters were discussed. It is expected that the model may offer useful guidance to the design and the performance improvement of MFIS structure devices.

2. Theory

2.1. Approach

To develop the model of MFIS structure, the switching physics of ferroelectric capacitor and the silicon physics of MOS structure

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Nomenclature

ε_0	permittivity of free space $\sim 8.854 \times 10^{-12}$ (F/m)	p_{p0}	equilibrium concentration of the hole in the semiconductor (m^{-3})
k_0	Boltzmann's constant $\sim 1.38 \times 10^{-23}$ (J/K)	A_I	area of the buffer layer (m^2)
T	absolute temperature (K)	A_F	area of the ferroelectric layer (m^2)
Q	charge unit $\sim 1.602 \times 10^{-19}$ (C)	V_I	voltage drops in the buffer layer (V)
n_{p0}	equilibrium concentration of the electron in the semiconductor (m^{-3})	V_F	voltage drops in the ferroelectric layer (V)

need to be considered simultaneously. For MOS structure, the capacitance is physically determined by the surface potential of silicon substrate, and the surface potential of silicon substrate is a function of the properties of oxide layer and silicon substrate [5]. However, for MFIS structure, the surface potential of silicon substrate is also affected by the polarization behavior of ferroelectric layer. The ferroelectric polarization behavior can be described by DST. Combined DST with the silicon physics of MOS structure, characteristics of MFIS structure such as the *C–V* characteristic and memory window can be modeled.

2.2. C–V equations of MFIS structure

The MFIS structure and its equivalent circuit are shown in Fig. 1. t_I and t_F are the thicknesses of the ferroelectric and the insulator layers. ε_I and ε_{Si} represent the relative constants of the insulator layer and the silicon substrate. In this paper, the MFIS structure is assumed ideal and there are no interface traps, space charge and other defects. Considering the continuous boundary condition of MFIS structure, the electric displacement vector **D** is given by

$$\mathbf{D} = \varepsilon_0 \mathbf{E}_F + \mathbf{P}(\mathbf{E}_F) = \varepsilon_I \varepsilon_0 \mathbf{E}_I = \varepsilon_{Si} \varepsilon_0 \mathbf{E}_{Si}, \tag{1}$$

where $\mathbf{E}_F$, $\mathbf{E}_I$, and $\mathbf{E}_{Si}$ are the electric fields in the ferroelectric layer, insulator layer, and silicon substrate, respectively. $\mathbf{P}(\mathbf{E}_F)$ is the ferroelectric polarization due to switching dipoles. The term $\varepsilon_0 \mathbf{E}_F$ can be neglected because it is much smaller than the term $\mathbf{P}(\mathbf{E}_F)$. According to Gauss Law, the relationship between the surface charge density of the semiconductor Q_{Si} and $\mathbf{E}_{Si}$ can be given by $Q_{Si} = -\varepsilon_{Si}\varepsilon_0 \mathbf{E}_{Si}$, and Eq. (1) can be rewritten as

$$\mathbf{P}(\mathbf{E}_F) = -Q_{Si}. \tag{2}$$

For p-type silicon, Q_{Si} is given by [10]

$$Q_{Si} = \mp \frac{2\varepsilon_{Si}\varepsilon_0 k_0 T}{qL_D} \times \left\{ \left[exp\left[-\frac{q\varphi_{Si}}{k_0 T} \right] + \frac{q\varphi_{Si}}{k_0 T} - 1 \right] + \frac{n_{p0}}{p_{p0}} \left[\left[exp\left[\frac{q\varphi_{Si}}{k_0 T} \right] - \frac{q\varphi_{Si}}{k_0 T} - 1 \right] \right] \right\}^{1/2}, \tag{3}$$

where φ_{Si} is the silicon surface potential and $L_D = \left(\frac{2\varepsilon_{Si}\varepsilon_0 k_0 T}{q^2 p_{p0}} \right)^{1/2}$ is Debye Length.

From Fig. 1, the total capacitance of MFIS structure is given by

$$C = \left(\frac{1}{C_I} + \frac{1}{C_F} + \frac{1}{C_{Si}} \right)^{-1}, \tag{4}$$

where C_I is the capacitance of insulator and defined by $\frac{A_I \varepsilon_I \varepsilon_0}{t_I}$. C_F is the capacitance of ferroelectric layer and given by $\frac{A_F \varepsilon_F \varepsilon_0}{t_F}$. C_{Si} is the capacitance of substrate and given by

$$C_{si} = \left| \frac{\partial Q_{si}}{\partial \varphi_{si}} \right| = \frac{\varepsilon_{Si}\varepsilon_0}{L_D} \frac{\left\{ \left[-exp\left(-\frac{q\varphi_{Si}}{k_0 T} \right) + 1 \right] + \frac{n_{p0}}{p_{p0}} \left[exp\left(\frac{q\varphi_{Si}}{k_0 T} \right) - 1 \right] \right\}}{\left\{ \left[\exp\left(-\frac{q\varphi_{si}}{k_0 T} \right) + \frac{q\varphi_{si}}{k_0 T} - 1 \right] + \frac{n_{p0}}{P_{p0}} \left[\exp\left(\frac{q\varphi_{si}}{k_0 T} \right) - \frac{q\varphi_{si}}{k_0 T} - 1 \right] \right\}^{1/2}}. \tag{5}$$

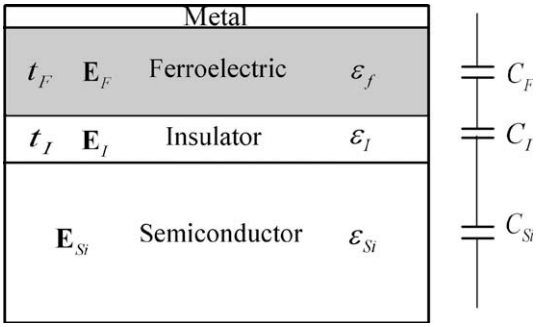

Fig. 1. Cross-sectional schematic of MFIS structure and its equivalent circuit.

The total voltage V_G applied on MFIS structure is described as follows:

$$V_G = \varphi_{Si} + V_I + V_F, \tag{6}$$

where $V_F = t_F E_F$, and V_I is given by Eqs. (1) and (2). The definition of relative parameters is given in the Nomenclature.

Eqs. (1)–(6) together completely describe the capacitor operation of MFIS structure when the polarization $\mathbf{P}(\mathbf{E}_F)$ is known. It should be noted that Eq. (5) is suitable only at low frequency. At high frequency, the capacitance of the MFIS structure at the inversion region does not follow Eq. (5) because the generation rate of the charge carriers from the depletion region can not follow the rapid change of the applied signal. We constrain the capacitance to the minimum value at the strong inversion condition, as the ordinary *C–V* is measured at high frequency.

2.3. Dipole polarization

The polarization behavior of ferroelectric layer is caused by the dipole switching. A ferroelectric capacitor containing a switching ferroelectric layer and two non-switching dielectric layers adjacent to the electrodes is shown in Ref. [3]. The non-switching dielectric layer is contributed by non-switching dielectrics of impurities, defects, and crystal interfaces, and its thickness is *d/2*. The ferroelectric layer thickness is *l*. For an ideal ferroelectric capacitor, *d* is simply zero.

When an electric field **E** is applied to the ferroelectric capacitor, the macro electric field, the polarization and the electric field contributed by the dipoles are $\mathbf{E}_f$, $\mathbf{P}_f$ and $\mathbf{E}_p$. $\mathbf{E}_f$ is equal to $\mathbf{E} - \frac{d}{l}\mathbf{E}_d$ [11], where $\mathbf{E}_d$ is the electric field of non-switching dielectric layer. The effective electric field acting on the dipoles is given by

$$\mathbf{E}_{eff} = \mathbf{E}_f + \mathbf{E}_p = \mathbf{E} - \frac{d}{l}\mathbf{E}_d + \mathbf{E}_p. \tag{7}$$

Because of the effect of $\mathbf{E}_{eff}$, a torque acting on the dipole tends to orient the dipole parallel to the field. All dipoles in the ferroelectric layer will be oriented parallel to the field and the polarization of the ferroelectric reaches its maximum value $\mathbf{P}_m$ only when the maximum external electric field $\mathbf{E}_m$ is higher than or equal to the