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RF performance of GaAs pHEMT switches with various upper/lower δ-doped ratio designs

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ABSTRACT

AlGaAs/InGaAs pseudomorphic high-electron-mobility transistor (pHEMT) single-pole-single-throw (SPST) switches with various upper/lower δ-doped ratio designs were fabricated and investigated for the first time. Both off-state capacitance and the specific on-resistance (R_{on}) of pHEMT are dominated factors and showed characteristics of sensitive to upper/lower δ-doped ratio for RF switch applications. By adopting the series-shunt architecture, upper/lower ratio of 3:1 switch achieved the lowest insertion loss compared to 4:1 design owing to the device shunt to ground (M2) of 4:1 design exhibited a worse fundamental signal isolation especially at high power level. As to the isolation under same architecture, however, due to the lowest R_{on} can be obtained, the 4:1 design provided better isolation performance. In addition, the M2 also dominated the second and third harmonics suppression and meanwhile, the lowest R_{on} of 4:1 design was found to be beneficial to the reduction of the harmonics power transmitted to the output terminal.

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1. Introduction

Transmitter and receiver switches have become important components in microwave system because of the growing demand for RF switches in time division duplexing systems such as wireless LAN and broadband systems. Complex switching functions, such as those required in 3G and 4G phones (SP5T or SP6T), are easier to be realized in GaAs pHEMT MMIC technologies than traditional MIC PIN diode technologies due to the faster switching speed. Furthermore, the lower power consumption of GaAs pHEMT switch increases the usage time of portable devices. However, the insertion loss of switch will affect the sensitivity of receiver and the output power of transmitter. Therefore, improving insertion loss of GaAs pHEMT switches in order to improve transceiver overall noise figure and output power has become an important requirement for commercial products [1,2]. In modern GaAs pHEMT industry, uniform doping profile in Schottky layer is widely replaced by planar δ-doped structure in order to obtain higher carrier injection efficiency into 2-DEG (two dimensional electron gas) [3]. In addition, compared to traditional single planar δ-doped design in pHEMTs, double planar δ-doped design achieved a higher current drive capability, wider dynamic range, and better linearity. Doping modifications in the Schottky layer (Schottky layer doped) and in the channel layer (channel doped) of the conventional δ-doped InGaP/InGaAs pHEMT have been investigated for amplifier applications [4]. However, the doping profiles discussed were not suitable for explaining the linearity of switch pHEMT because the RF switches were only operated at on-state and off-state. The voltage drops between drain and source terminals were usually small. The maximum transmit power of conventional series-shunt pHEMTs switches is directly related to the RF voltages swing across the drain-source and gate of the off-state pHEMTs. High power and low distortion switch operation can only be achieved by higher pinch-off voltage pHEMT, higher control voltage and uniform off-state capacitance distribution of pHEMTs. To increase the pinch-off voltage will sacrifice the switch R_{on} performance and result in a higher insertion loss due to shallow channel profile [5]. In order to obtain the low R_{on} and enhanced pinch-off voltage of pHEMT simultaneously, this report investigated various upper/lower δ-doped ratio designs systematically. The RF switch performance with optimum upper/lower δ-doped ratios was then demonstrated.

2. Device structure and fabrication

Fig. 1 shows the epitaxy structure of double heterostructure Si δ-doped pHEMTs with various upper/lower δ-doped designs. Two Si planar δ-doped layers sandwiched the 12 nm InGaAs undoped channel layer for high power consideration. Then the n^- doped

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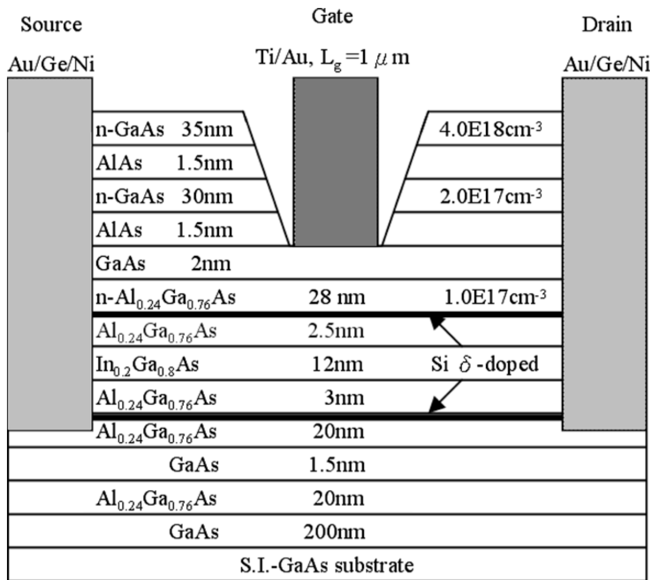


Fig. 1. The cross-sectional structure of 1 μm-long gate double Si δ-doped AlGaAs/InGaAs pHEMTs.

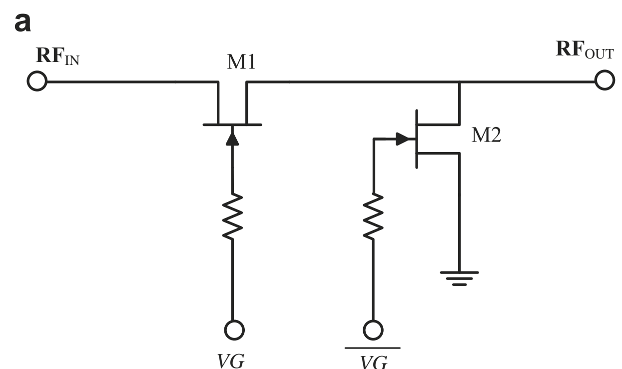
28 nm AlGaAs layer was grown beneath 2 nm intrinsic GaAs for Schottky layer, which is beneficial for avoiding the AlGaAs exposed in the moisture after gate recess process. Finally, a double recess cap layer design consisted of a 30 nm n^--GaAs and a 35 nm n^+-GaAs was grown on the Schottky layer. The upper Si δ-doped layer is doped with four different concentrations, i.e., $1 \times 10^{12}\,cm^{-2}$, $2 \times 10^{12}\,cm^{-2}$, $3 \times 10^{12}\,cm^{-2}$ and $4 \times 10^{12}\,cm^{-2}$, respectively, and the lower Si δ-doped concentration is kept at $1 \times 10^{12}\,cm^{-2}$. The lower Si δ-doped concentration for pHEMTs is to maintain both gate-to-channel control ability and suitable pinch-off voltage, because these effects are very sensitive to the δ-doped concentration when layer is far away from gate electrode. Devices were processed by conventional optical lithography and lift-off technology. Ohmic contacts were realized by using Au/Ge/Ni alloy followed by a 430 °C, 2 min RTA annealing in N_2 ambient. In order to define an active region and switch device, an $NH_4OH/H_2O_2/H_2O$ solution was used for 200 nm depth mesa etching solution. As to the critical gate-recessed process, a high selective succinic acid solution was applied for high uniformity consideration and then a Ti/Au metal gate was deposited for gate electrode [6]. After a surface treatment, a 150 nm SiO_2 was deposited on the devices, and via holes connecting all the source pads were defined by photolithography. Finally, a 1 μm thick top Au layer was evaporated for bridging the source pads and interconnections.

3. Results and discussion

Several 1.0 μm-long gate AlGaAs/InGaAs double heterostructure Si δ-doped pHEMTs on GaAs substrate with various upper/lower δ-doped were evaluated on-wafer. The R_{on} values were 6.8 Ω mm, 4.1 Ω mm, 2.9 Ω mm and 2.3 Ω mm for upper/lower δ-doped ratio from 1:1 to 4:1 designs, respectively. The higher upper δ-doped concentration achieved a lower R_{on} which is beneficial for improving device current density and switches insertion loss. The maximum drain-to-source current ($I_{d\ max}$) was also achieved at the higher upper δ-doped concentration. The current density values were 240 mA/mm, 345 mA/mm, 475 mA/mm and 541 mA/mm from 1:1 to 4:1 designs, respectively. In addition, by defining the device pinch-off voltage (V_p) at I_{ds} of 1 mA/mm, the higher upper δ-doped design performed a deeper V_p. The pinch-off voltages were −0.3 V, −0.7 V, −1.1 V and −1.2 V from 1:1 to 4:1 designs, respectively. Table 1 listed the intrinsic parameters of various devices by extracting the measured *S*-parameters. The gate-to-source capacitance (C_{gs}) increased with the upper δ-doped concentration owing to the suppression of depletion layer at the high doping profile. Therefore, the thin depletion region of high upper δ-doped concentration provided a lower isolation characteristic and the depletion region distribution was influenced easily at high power swing. However, no obvious changes were found at gate-to-drain capacitance (C_{gd}) and drain-to-source capacitance (C_{ds}) with various upper/lower δ-doped designs. The channel resistance (R_i) and intrinsic transconductance (g_{mi}) both showed the same trends with their dc performance. The transit time was also improved following with the upper δ-doped concentration which was beneficial for improving the switch charge and discharge delay time for RF switch applications. To achieve high power handling capability and low harmonics for SPST switch circuits, the series-

Table 1
The intrinsic parameters of various upper/lower δ-doped ratio designs.

Parameters	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_i (Ω)	g_{mi} (mS)	τ (ps)
1:1	197.1	23.43	33.24	31.31	14.53	5
2:1	213.4	26.35	34.32	6.32	18.82	4.2
3:1	327.9	24.66	35.76	6.12	24.32	4
4:1	364.3	21.95	35.8	6.17	29.66	3.9



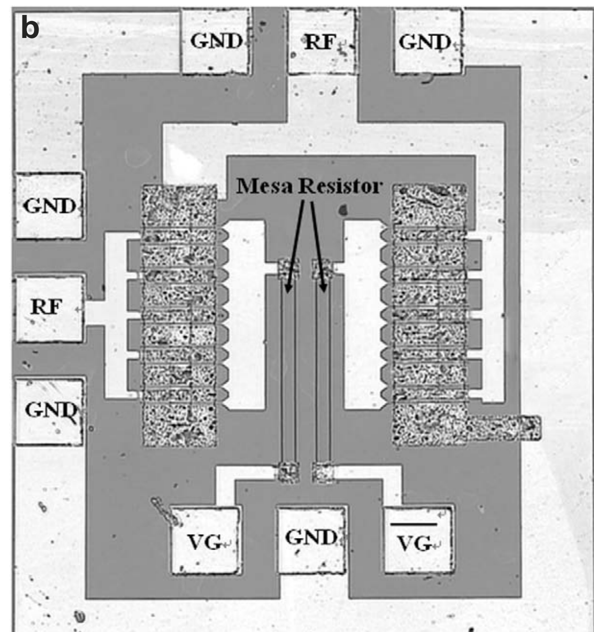


Fig. 2. The series-shunt SPST switch, (a) circuit diagram and (b) chip photography.

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