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Analytical threshold voltage model for lightly doped short-channel tri-gate MOSFETs

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ABSTRACT

A simple analytical threshold voltage model for lightly doped tri-gate MOSFETs has been developed, using the superposition of the threshold voltages of a symmetric and an asymmetric double-gate MOSFET. The model has been verified by comparison with experimental and simulation results of tri-gate FinFETs with various fin widths and channel lengths. Excellent agreement between model, experimental and simulation results is obtained, demonstrating the validity of the proposed threshold voltage model.

1. Introduction

Tri-gate (TG) MOSFETs, like FinFETs, are considered to be the best candidates for sub-100 nm scaling of MOSFETs due to their multi-gate immunity to short channel effects (SCEs), proximity to standard bulk planar CMOS processing, feasibility for digital/analogue circuit applications and low power consumption [1–8]. Little work has been done towards the development of analytical expression for the threshold voltage of TG MOSFETs which is usually not fully analytical [9,10], whereas no experimental data were used to verify its validity. In this work, we develop a fully analytical model for the threshold voltage of lightly doped TG MOSFETs, which is compared with experimental results showing excellent agreement.

2. Threshold voltage formulation

A schematic view of the TG transistor cross-section is shown in Fig. 1, where the channel is lightly doped silicon with acceptor concentration N_a. H_{fin} is the fin thickness, W_{fin} is the fin width and L is the channel length. The gate electrode surrounds the silicon body on three sides with a gate oxide of thickness t_{ox} and the bottom oxide thickness is t_{oxb}. The gate material is a metal with a proper work function for adjusting the threshold voltage. V_{gs} represents the voltage applied to the gate, V_{gsb} the voltage applied to the bottom gate and V_{ds} the voltage applied to the drain.

The TG MOSFET consists of two independent double-gate (DG) MOSFETs, a symmetric between the two lateral gates and an asymmetric one between the top and bottom gates. The three-dimensional potential distribution along the channel has been derived in weak inversion based on a perimeter-weighted approach of the potential distributions of the symmetric and asymmetric DG MOSFETs [11]. Following [12], the threshold voltage of the TG MOSFET can be obtained by the superposition of the threshold voltage of the symmetric and asymmetric DG MOSFETs.

The threshold voltage of a transistor can be defined as the gate voltage at which the minimum carrier charge sheet density of the inversion charge Q_{inv} reaches a value Q_{th}, adequate to achieve the turn-on condition at the position of the minimum potential along the channel length (y-axis), usually referred as "virtual cathode" [13]. For a short-channel TG MOSFET, in weak inversion the position of the most leaky path starts to form first at the bottom center of the channel and in strong inversion the most leaky path moves to the corner regions where maximum gate control is achieved [14]. The corner effect can have a severe influence on the electrical characteristics of short-channel TG devices, resulting in a hump in the plots of the transconductance around the threshold and an increase of the corner threshold voltage [14]. This movement of the most leaky path within the channel cross-section must be taken into account in deriving the drain current equation in short TG

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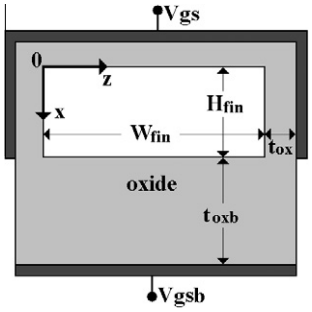

Fig. 1. Cross-section of a TG MOSFET.

FinFETs [14]. Adopting that in TG MOSFETs in weak inversion the most leaky path is located at the middle of the bottom surface of the channel for $x = H_{fin}$ and $z = W_{fin}/2$ [10] and based on the potential distribution presented in [11], the threshold voltage of the lightly doped symmetric DG MOSFET can be expressed as follows [15]:

$$V_{t,sym} = \varphi_{ms} + A(\lambda_{sym})V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 W_{fin}}\right) - B(\lambda_{sym})(2V_{bi} + V_d) - C(\lambda_{sym})\left[V_{bi} - V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 W_{fin}}\right)\right]^{1/2} \times \left[V_{bi} + V_d - V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 W_{fin}}\right)\right]^{1/2}, \quad (1)$$

where V_{th} is the thermal voltage and λ_{sym} is the natural length of the symmetric DG MOSFET given by:

$$\lambda_{sym} = \sqrt{\frac{\varepsilon_{Si} t_{ox} W_{fin}}{4\varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{W_{fin}}{4t_{ox}}\right)}. \quad (2)$$

ε_{Si} is the dielectric constant of silicon, ε_{ox} is the dielectric constant of the oxide, $V_{fb} = \varphi_{ms} - V_{th}\ln(N_a/n_i)$, φ_{ms} is the gate work function referenced to the silicon and $V_{bi} = V_{th}\ln(N_a N_d/n_i^2)$ is the built-in potential across the source/drain-channel junctions, with N_α the donor concentration of the channel, N_d the donor concentration of the source/drain contacts and n_i the intrinsic carrier concentration.

Following similar analysis as in [15] for symmetric DG MOSFETs, the threshold voltage of the asymmetric DG MOSFET can be expressed as follows:

$$V_{t,asym} = K_2 + \frac{A(\lambda_{asym})}{K_1}V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 H_{fin}}\right) - \frac{B(\lambda_{asym})}{K_1}(2V_{bi} + V_d) - \frac{C(\lambda_{asym})}{K_1}\left[V_{bi} - V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 H_{fin}}\right)\right]^{1/2} \times \left[V_{bi} + V_d - V_{th}\ln\left(\frac{N_a Q_{th}}{n_i^2 H_{fin}}\right)\right]^{1/2}, \quad (3)$$

where

$$K_1 = \frac{\varepsilon_{Si} t_{oxb}}{\varepsilon_{Si}(t_{ox} + t_{oxb}) + \varepsilon_{ox} H_{fin}}, \quad (4)$$

$$K_2 = \frac{[q(\varepsilon_{Si}/\varepsilon_{ox})N_a t_{ox} t_{oxb} H_{fin}] + [\varepsilon_{Si}\varphi_{ms}(t_{ox} + t_{oxb}) - \varepsilon_{ox}(H_{fin}V_{gsb} - \varphi_{ms}H_{fin})]}{\varepsilon_{Si}(t_{ox} + t_{oxb}) + \varepsilon_{ox}H_{fin}} - \frac{[\varepsilon_{Si} t_{ox} V_{gsb} - \frac{1}{2}qN_a H_{fin}^2 t_{oxb}]}{\varepsilon_{Si}(t_{ox} + t_{oxb}) + \varepsilon_{ox}H_{fin}}, \quad (5)$$

and λ_{asym} is the natural length of the asymmetric DG MOSFET given by:

$$\lambda_{asym} = \frac{1}{2}\sqrt{\frac{\varepsilon_{Si} t_{oxb} H_{fin}(2\varepsilon_{Si} t_{ox} + \varepsilon_{ox} H_{fin})}{\varepsilon_{ox}[\varepsilon_{Si}(t_{ox} + t_{oxb}) + \varepsilon_{ox}H_{fin}]}}. \quad (6)$$

In Eqs. (1) and (3), the parameters A, B and C are given by:

$$A(\lambda) = \frac{e^{\frac{4L}{\lambda}} - 2e^{\frac{2L}{\lambda}} + 1}{\left(e^{\frac{L}{\lambda}} - 1\right)^4}, \quad B(\lambda) = \frac{2e^{\frac{3L}{\lambda}} - 4e^{\frac{2L}{\lambda}} + 2e^{\frac{L}{\lambda}}}{\left(e^{\frac{L}{\lambda}} - 1\right)^4}, \quad C(\lambda) = \frac{2e^{\frac{L}{2\lambda}}\left(1 + e^{\frac{L}{\lambda}}\right)}{\left(e^{\frac{L}{\lambda}} - 1\right)^2}, \quad (7)$$

where $\lambda = \lambda_{sym}$ and $\lambda = \lambda_{asym}$ for the symmetric and asymmetric DG MOSFETs, respectively.

Auth and Plummer [12] have fully justified that the threshold voltage of a surrounding-gate MOSFET can be derived by the superposition of two independent devices, a cylindrical gate MOSFET and a symmetric DG MOSFET; the threshold voltage of the surrounding-gate MOSFET can be calculated as the perimeter-weighted sum of the threshold voltages of the cylindrical and the symmetric DG MOSFTs. Following the same concept, the threshold voltage of the TG MOSFET can be expressed as the perimeter-weighted sum of the threshold voltages of the symmetric and the asymmetric DG MOSFET as follows:

$$V_t = \frac{2H_{fin}}{W_{fin} + 2H_{fin}}V_{t,sym} + \frac{W_{fin}}{W_{fin} + 2H_{fin}}V_{t,asym.} \quad (8)$$

It is mentioned that Eq. (8) is analogous to what is done to describe the mobility behavior in FinFETs as a weighted average of the top and sidewalls mobility due to the anisotropy in effective masses [16,17].

3. Experimental verification of the model

The threshold voltage model has been verified by comparing the model with the experimental results obtained from 5-channel triple-gate FinFETs with variables parameters being the fin thickness and width. The devices were fabricated at IMEC (Leuven) on SOI wafers with 145 nm buried oxide thickness. The structure of the measured devices is shown in Fig. 2. The channel doping concentration is $N_a = 10^{15}\,cm^{-3}$. As gate insulator, HfO_2 was deposited by atomic layer deposition (ALD) with equivalent gate oxide thickness 1.7 nm, whereas 5 nm thick of ALD TiN film capped with 100 nm polysilicon was used as gate electrode. The dimensions of the devices are defined as following: The length of the spacer between gate and the large source/drain pads is 50 nm, the doping concentrations of the source/drain contacts and the spacers are about 2×10^{20} and $5 \times 10^{19}\,cm^{-3}$, respectively and the fin thickness H_{fin} is kept constant at 65 nm. Two fin widths were used $W_{fin} = 25$ and 55 nm with different gate lengths. The static transfer characteristics of the transistors at $V_d = 20$ mV and 1.02 V were measured at room temperature at wafer level using a SussMicroTec LT probe station and an HP 4155 semiconductor parameter

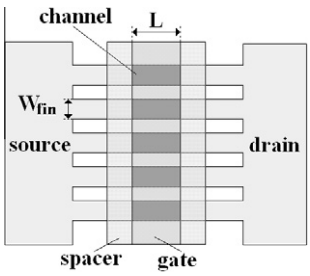

Fig. 2. Schematic presentation of the 5-fin triple-gate FinFET structure.