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Origin of flat band voltage shift in HfO_2 gate dielectric with La_2O_3 insertion

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ABSTRACT

The origin of flat band voltage (V_{FB}) shift with La_2O_3 insertion for HfO_2 gate dielectrics has been carefully examined. By separating the effect of the fixed charges located at each interface by thickness-dependent V_{FB} evolution, total voltage shifts (dipole) at metal/high-k and high-k/SiO_2 interfaces have been estimated. Using stacked capacitors of La_2O_3 and HfO_2, it can be concluded that V_{FB} is mainly determined by the high-k on SiO_2. Therefore, the dipole at La_2O_3 and the interface has an additional dipole of 0.36 eV compared with that of HfO_2/SiO_2. The same trend has also been obtained with a high-k on a Si substrate without a SiO_2 layer. A simple model using electronegativity has been proposed to explain the V_{FB} shift.

1. Introduction

While Si-based oxide films have been used as a gate dielectric for more than 30 years, further thinning of these films has already reached its limit owing to a large direct tunneling current [1]. Therefore, alternative gate dielectrics with a high permittivity (high-k) have been extensively examined [2]. Among them, Hf-based oxides, such as HfSiON, have been one of the promising candidates for next-generation gate dielectrics, owing to their high permittivity with a wide band gap and a good thermal stability. One of the issues of HfO_2-based materials is the difficulty in controlling the threshold voltage (V_{th}), as a relatively high V_{th} is obtained irrespective of the type of electrode used [3]. It has also been reported that the choice of a high-k has a large impact on V_{th} shift, for example, an ultra-thin La_2O_3 capping layer on a HfO_2 layer can negatively shift V_{th} to an ideal nMOSFET value [4]. On the other hand, the atomic composition of $HaLaO_x$ also showed a large impact on flat band voltage (V_{FB}) shift in capacitance–voltage (CV) characteristics [5]. Recently, it has been reported that a dipole at the $HfLaO_x/SiO_2$(IL) interface plays an important role in determining V_{FB} [6,7].

In this study, firstly, the relative voltage shifts existing at metal/high-k and high-k/SiO_2 interfaces are estimated using a thickness-dependent V_{FB} relation. Then, the V_{FB} value of stacked oxides of La_2O_3 and HfO_2 with various thickness orders are examined to observe the V_{FB} shift and to clarify which interface is dominant for the V_{FB} shift. Finally, the origin of the V_{FB} shift at an interface is explained by electronegativity.

2. Experimental methods

2.1. Device fabrication

Fig. 1 shows the fabrication flow of MOS capacitors. High-k dielectrics were deposited on a 300-nm-thick SiO_2 isolated *n*-Si(100) wafer with a thermally grown interfacial oxide layer (IL) with a thickness of 3.5 nm. HfO_2 and La_2O_3 were deposited by electron beam evaporation with an O_2 partial pressure of 10^{-4} Pa. The substrate temperature during the deposition was set to be 300 °C and the deposition rate of the high-k dielectrics was controlled to be 0.3 nm/min. After high-k deposition, 60-nm-thick tungsten (*W*) was *in situ* deposited by sputtering without exposing the wafers to air to prevent moisture or carbon absorption. *W* was patterned by reactive ion etching (RIE) using SF_6 chemistry to form a gate electrode for the MOS capacitors. The wafers were then post-metallization annealed (PMA) in a rapid thermal annealing (RTA) furnace in forming gas (FG) (N_2:H_2 = 97%:3%) ambient at 420 °C for 30 min. Back surface Al was deposited as a bottom electrode by thermal evaporation. CV characteristics of the MOS capacitors were measured at 100 k and 1 MHz using an Agilent 4284A precision LCR meter. The thickness of IL (3.5 nm) is chosen to be sufficient for suppressing the formation of oxygen vacancies in high-k dielectrics [8]. Moreover, as the annealing temperature studied in this work is low, the effect of Fermi level pining on V_{FB} can be neglected.

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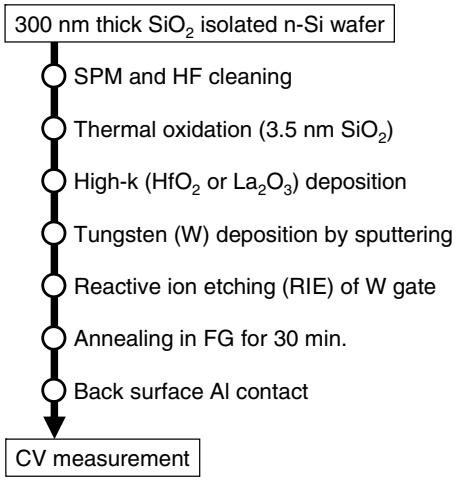

Fig. 1. Fabrication flow of MOS capacitors.

2.2. Estimation of fixed charges and dipoles at each interface

Fixed charges and dipoles presented at each interface in a simple SiO_2/Si MOS structure can be expressed with equivalent oxide thickness (EOT) and V_{FB} as [9]

$$V_{FB} = -\mathrm{EOT}\left(\frac{Q_0}{\varepsilon_0\varepsilon_{ox}}\right) + \frac{\varphi_{ms}}{q} + \left(\Delta_{metal/SiO_2} + \Delta_{SiO_2/Si}\right), \quad (1)$$

where Q_0 is the fixed charge at the SiO_2/Si interface, φ_{ms} is the difference between work functions of the metal and Si substrate, and Δ_{metal/SiO_2} and $\Delta_{SiO_2/Si}$ are dipoles at the metal/SiO_2 and SiO_2/Si interfaces, respectively. The fixed charges inside the oxide layer are neglected as the effects of these charges are small. When a SiO_2 IL with a thickness of EOT_{IL} is inserted under a high-k oxide, Eq. (1) can be modified as

$$V_{FB} = -\mathrm{EOT}\left(\frac{Q_0 + Q_1}{\varepsilon_0\varepsilon_{ox}}\right) + \frac{Q_1 \cdot \mathrm{EOT}_{IL}}{\varepsilon_0\varepsilon_{ox}} + \frac{\varphi_{ms}}{q} + \left(\Delta_{metal/high\text{-}k} + \Delta_{high\text{-}k/IL} + \Delta_{IL/Si}\right). \quad (2)$$

Here, Q_1 is the fixed charge located at the high-k/SiO_2 interface and $\Delta_{metal/high\text{-}k}$ and $\Delta_{high\text{-}k/SiO_2}$ are dipoles at the metal/high-k and high-k/SiO_2 interfaces, respectively. A schematic model of the charge locations and dipoles in a metal/high-k/SiO_2/Si stack is illustrated in Fig. 2.

3. Results

3.1. Fixed charges and dipole extraction of HfO_2/SiO_2 and La_2O_3/SiO_2 capacitors

Fig. 3 shows the CV characteristics of MOS capacitors with different HfO_2 or La_2O_3 thicknesses on SiO_2 IL (3.5 nm). The thicknesses of La_2O_3 and HfO_2 vary from 5 to 10 nm. Capacitors with different SiO_2 thicknesses are also shown. It is clear that the V_{FB} values of the CV curves with HfO_2/IL stacks reside in the positive direction compared with those of SiO_2 and La_2O_3/IL stacks. Fig. 4 shows the V_{FB}-EOT plot of the fabricated HfO_2/SiO_2/Si and La_2O_3/SiO_2/Si stacks. Using Eq. (1), a Q_0 of -1.7×10^{12} cm^{-2} is obtained for SiO_2 capacitors. Thus, the Q_1 values for La_2O_3 and HfO_2 using Eq. (2) are estimated to be 1.6×10^{12} and -2.8×10^{12} cm^{-2}, respectively. In this calculation, the presence of a La–silicate layer, which was confirmed by transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS), was neglected as the effect of such presence on V_{FB} was small.

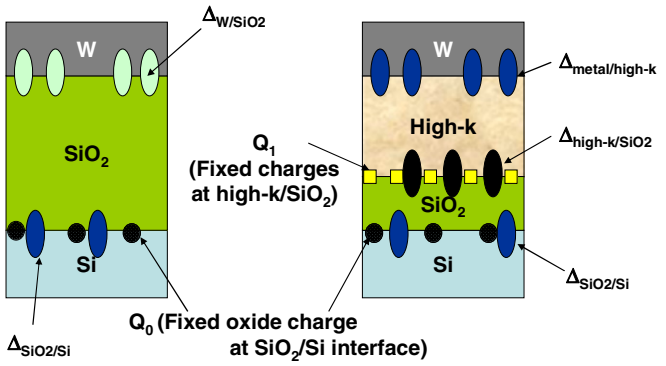

Fig. 2. Schematic model of fixed charges and dipole locations used in Eqs. (1) and (2).

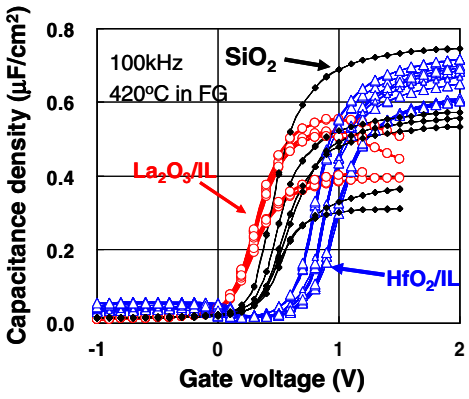

Fig. 3. CV curves of HfO_2/SiO_2/Si and La_2O_3/SiO_2/Si with different high-k thicknesses. Capacitors with different SiO_2 thicknesses are also shown.

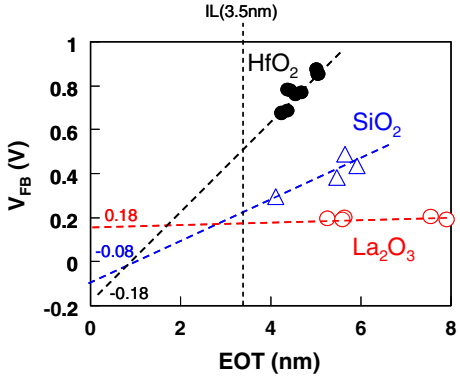

Fig. 4. V_{FB}-EOT plot of fabricated HfO_2/SiO_2/Si and La_2O_3/SiO_2/Si stacks.

The difference in total dipole between the capacitors, which is the difference between $q(\Delta_{W/HfO_2} + \Delta_{HfO_2/IL})$ and $q(\Delta_{W/La_2O_3} + \Delta_{La_2O_3/IL})$, is calculated to be 0.36 eV. The dipole differences at the W/high-k interface cannot be separated at this point. In the next subsection, this contribution will be discussed using stacked MOS capacitors.

3.2. Flat band voltage behavior on stacked high-k MOS capacitors

To separate the contribution of metal/high-k and high-k/SiO_2 from the obtained total dipole difference, capacitors with La_2O_3 and HfO_2 stacks with various thicknesses and stacking orders were