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Effect of high-energy neutrons on MuGFETs

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ABSTRACT

This paper investigates, for the first time, the influence of high-energy neutrons on Multiple-Gate FETs (MuGFETs) with various gate lengths and fin widths. Neutron-induced degradation is addressed through the variation of major device parameters such as threshold voltage, subthreshold slope, maximum transconductance and DIBL. We demonstrate that high-energy neutrons result in total-dose effects largely similar to those caused by γ- and proton-irradiations. It is shown that, contrarily to the generally-believed immunity to irradiation, very short-channel MuGFETs can become extremely sensitive to the total-dose effect. The possible reasons of such length-dependent neutron-induced degradation are discussed and finally related to gate edges.

1. Introduction

Multiple-Gate FETs (MuGFETs) are widely recognized as one of the promising candidates to satisfy the ITRS requirements for the future nanoscaled device generations, due to the improved control of the channel from the gates [1]. Moreover, they seem to be very attractive for aerospace applications thanks to their predicted higher temperature stability [2] and radiation hardness [3–7]. Such perspectives motivate a large number of investigations of both total dose and transient radiation effects in these devices.

Previously reported studies investigate γ- or proton-irradiations [3–6] and effect of heavy-ions [7] on MuGFETs, while effect of neutrons is generally considered as negligible or secondary. However, at avionics altitudes, for instance, the neutron component of the secondary cosmic radiation is about half of the dose equivalent [8] with the maximum of the total neutron flux at 15–20 km above sea level [9]. Nevertheless, even at sea level, cosmic rays consist in about 10% of neutrons [9]. Neutrons in a wide energy range from 0.1 eV to more than 1 GeV are present. The measured neutron spectra for avionics altitudes [8,10] exhibit almost no thermal neutrons, a large peak near 1 MeV and a second broad peak near 100 MeV. The shape of spectrum varies only slightly for altitudes of 12–21 km above sea level, while at the sea level higher thermal neutron component appears (due to backscattering from the terrestrial surface) [8,9]. Furthermore, neutrons are highly present in a nuclear reactor environment [11] as well as in High Energy Physics large scale experiments (at CERN, for example), where among the most serious problems is the massive neutron background produced by hadronic interactions [12]. Neutron background leads to the destruction of detectors and readout electronics, thus limiting the devices lifetime.

It is widely considered that since neutrons are uncharged particles, their main effect is non-ionizing or displacement damage whereas they cannot interact directly with charged particles to ionize them [11]. When neutron strikes solids, it may transfer enough energy to atom so that to displace from site within the crystal lattice structure. This atom, named a primary knock-out (or recoil) atom can, in turn, displace other lattice atoms, thus producing cascade reaction. Number of created lattice defects (vacancies and interstitial atoms) degrades the material quality reducing lifetime, mobility values, diffusion length, etc. Displacement damages are considered to be primarily important for bipolar devices strongly decreasing their gain, while MOS devices are known to be tolerant to displacement-caused degradation up to neutron fluencies of 10^{15} n/cm^2 [11]. Even if major effect of neutrons on solids is

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displacement damage, neutrons are believed to be capable to produce ionization damages through indirect or secondary processes, e.g. ionization by sufficiently energetic recoil atom or non-elastic interaction between neutron and nucleus, followed by proton or α-particle emission [11]. Neutron-induced effects in CMOS circuits receive increase attention during last years [9,13–16]; particularly, neutron-induced Single-Event Upsets are widely considered [9,13,14]. Additionally, Vaidya et al. [15] demonstrates that neutrons can induce positive charge accumulation in oxides and interface charge build-up and [16] shows that neutron can produce electronic damage in the gate oxide which resembles that created by γ-rays.

In this work we will show, for the first time to our best knowledge, that high-energy neutrons cause total-dose effects (build-up of interface states and positive oxide charges) in MuGFETs, which are largely similar to the total-dose effects due to γ- or proton-irradiation reported previously [3–6].

Next, most of the previous studies are focused on radiation hardness advantages of relatively long-channel MuGFETs comparing to their wide-fin quasi-planar counterparts. These works clearly demonstrate much higher immunity of narrow-fin MuGFETs to the total-dose effects comparing to the quasi-planar FD SOI MOSFETs with almost zero parameters degradation when irradiated up to 6 Mrad [3–6]. In our paper we analyze the devices with gate lengths down to 50 nm and point out the influence of channel length on the neutron-induced MuGFETs parameters degradation. Such important parameters as subthreshold slope (S), threshold voltage (V_T), drain-induced barrier lowering (DIBL) and transconductance maximum ($G_{m\ \max}$) are considered.

2. Experimental details

Tri-gate FinFETs with Ω-configuration and mid-gap metal gate electrodes were fabricated at IMEC on SOI wafers with 60 nm film and 145 nm buried oxide (BOX). The active area fins were patterned using 193-nm optical lithography with resist and oxide hard mask trimming. Hydrogen annealing and sidewall oxidation were used for surface smoothening and corner rounding [17]. An ALD HfO_2 deposited on chemical oxide with total effective oxide thickness of 1.4 nm was used as the gate dielectric. A mid-gap MOCVD TiN was used as the gate electrode. The metal was capped with 100 nm poly. As and BF2 extensions were implanted with high angle and 45 nm PECVD nitride spacers were formed. No selective epitaxial growth was used to reduce the source/drain resistance. After spacer etch, HDD implantations were done, followed by a spike anneal and a standard NiSi process and Cu BEOL metallization. Devices under study are 1-fin and 5-fins n- and p-channel FETs with a fin height of 60 nm, gate length, L, varying from 50 nm to 10 μm and fin widths, W_{fin}, from 25 nm to 3 μm. The silicon body in these devices was left undoped and hence the 1–3 μm wide fin FinFETs can be considered as a quasi-planar FD SOI MOSFETs.

Neutron irradiation was performed at neutron irradiation facility (NIF) at CYCLONE, Louvain-la-Neuve, Belgium. A fast neutron beam with high neutron flux was used; the produced neutrons have an energy spectrum from 5 to 45 MeV with a peak in a region of 20 MeV [18]. Neutrons in this energy range are widely present at avionics altitudes [8–10], at the sea level [9], as well as with lower percentage at nuclear reactors and at LHC [19–21]. Therefore, though the neutron-induced effects in semiconductor devices depend on the neutron energy, the neutrons with energies used in this work are of interest for a number of applications.

The devices were irradiated up to the fluencies of $\sim 2.2 \times 10^{12}$, 2.2×10^{13} and 2.2×10^{14} n/cm^2, which corresponds to the dose equivalent of 10^4, 10^5 and 10^6 rad (alanine). The concomitant γ-rays, always present during neutron irradiation, is only 2.4% (+0.03% of light particles) in our case [18,22]. Irradiation was performed in a passive regime, i.e. without application of any bias during irradiation. While it is not the worst-case condition, it allows building a first insight on the physical device behaviour.

3. Experimental results

Fig. 1a presents I_dV_g curves for 10 μm-long devices with different fin widths from 3 μm down to 25 nm before and after neutron irradiation with dose of 10^6 rad. A strong shift of curves to negative gate voltages, which increases with W_{fin}, is observed in wide-fin quasi-planar devices, which is essentially similar to previously reported data for the wide-fin MuGFETs irradiated with γ-rays and protons [5,6]. Such behaviour is indeed typical for irradiated FD SOI MOSFETs and explained by the activation of the back channel caused by the radiation-induced positive charge accumulation in the BOX. Fig. 1b shows second derivative of drain current for the devices with different W_{fin} clearly indicating the appearance of two maxima, i.e. front and back threshold voltages, for the wide-fin devices. The 2.4% of concomitant γ-rays present during our neutron irradiation are too small to be able to explain the observed effect. The most probable reason is ionization by secondary processes as mentioned above. Different knock-out reaction can be imagined to be responsible for the BOX charge build-up in the complex system containing different composite materials (as oxides, nitrides, metals). For the 20 MeV neutrons, the largest cross section values (among the elements/compounds present in our structures) were reported for their interaction with Hf, W, Si_3N_4, HfO_2 [9,23]. However, this information is not sufficient to conclude that these reactions are responsible for the observed effects, because the energy of secondary particle as well as its location has to be taken into account. In [14] it was shown that e.g. W and Ta being secondary ions produced with rather high probability, have very low energy and do not reach sensitive volume of SRAM, though WSi_2 is contacted to it. Furthermore, neutrons are known to ionize more easily the materials containing high hydrogen concentration [11]. The buried oxide of SOI structures was shown to contain high hydrogen concentration after some process steps [24]; additionally hydrogen annealing was used for fin smoothing and corner surrounding in our FinFET processing. Detailed Monte-Carlo simulations for concrete structure and neutron energies are necessary to distinguish most probable reaction, which, however, is out of scope of this paper.

Fig. 2a shows the variation of threshold voltage before and after irradiation with different doses as a function of fin width. It is seen, that negative threshold voltage shift as high as 0.5 V is observed for the wide-fin devices. In the same time, long-channel narrow-fin devices stay unaffected by neutron irradiation. Indeed, thanks to the strong lateral gates coupling, inner to the narrow MuGFETs, the back channel activation almost does not affect I_dV_g curves and V_T for the devices with $W_{\text{fin}} < 125$ nm in our case (Figs. 1 and 2a).

Fig. 2b shows variation of neutron-induced V_T shift as a function of L for both narrow- and wide-fin devices; for wide-fin devices only the shift of front threshold voltage is considered. It is seen that, surprisingly, V_T shift becomes positive for the short-channel devices and, moreover, increases with L decrease, reaching about 100 mV for the shortest device. One might say, that positive shift of threshold voltage can be attributed to the exotic negative charge build-up in the high-k gate dielectric. However, if it was a plausible reason, positive V_T shift would be observed for any device length, which is not the case for our observations. In our case, positive versus negative threshold voltage shift is probably a result of competing effect of positive charge build-up in gate dielectric and in BOX and negatively-charged interface traps on the 2D-fin structure as