Solid-State Electronics 52 (2008) 1018–1023

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Comparison of heterostructure-emitter bipolar transistors (HEBTs) with InGaAs/GaAs superlattice and quantum-well base structures

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ARTICLE INFO

Article history:
Received 19 July 2007
Received in revised form 11 January 2008
Accepted 25 February 2008
Available online 8 April 2008

The review of this paper was arranged by Prof. Y. Arakawa

Keywords:
InGaP/GaAs
Heterostructure-emitter
Superlattice-base
Quantum-well base
Turn-on voltage
Offset voltage

ABSTRACT

The characteristics of InGaP/GaAs heterostructure-emitter bipolar transistors (HEBTs) including conventional GaAs bulk base, InGaAs/GaAs superlattice-base, and InGaAs quantum-well base structures are presented and compared by two-dimensional simulation analysis. Among of the devices, the superlattice-base device exhibits a highest collector current, a highest current gain and a lowest base–emitter turn-on voltage attributed to the increased charge storage of minority carriers in the InGaAs/GaAs superlattice-base region by tunneling behavior. The relatively low turn-on voltage can reduce the operating voltage and collector–emitter offset voltage for low power consumption in circuit applications. However, as to the quantum-well base device, the electrons injecting into the InGaAs well are blocked by the p^+-GaAs bulk base and it causes a great quantity of electron storage within the small energy-gap n-type GaAs emitter layer, which significantly increases the base recombination current as well as degrades the collector current and current gain.

1. Introduction

Heterojunction bipolar transistors (HBTs) have attracted significant interest of high-speed digital and microwave circuit applications due to their superior performance [1,2]. However, the conventional HBTs suffered from a large collector–emitter offset voltage (ΔV_{CE}) resulting from a considerable base–emitter (B–E) turn-on voltage, which severely limits the minimum operated voltage and causes high power consumption in circuit applications [3,4]. It is well known that two usual approaches, i.e., the reduction of potential spike at B–E junction [5–7] and the employment of a small energy-gap material as base layer [8–10], have been used for the reduction of the turn-on voltage.

First, in order to decrease the potential spike at B–E junction, some improved npn transistors, e.g., setback HBTs [5] and heterostructure-emitter bipolar transistor (HEBTs) [6,7], have been addressed and fabricated. As to the setback HBTs, an undoped setback layer added at B–E junction is entirely depleted and helps to lower the energy-band at the emitter side. However, the potential spike might be not completely eliminated unless the setback layer is thick enough. Then, it will result in large spacer recombination current and degrade the current gain [5]. For the HEBTs, a small energy-gap n-type emitter layer is added at B–E junction for reducing the potential spike and offset voltage. Nevertheless, if the small energy-gap emitter layer is too thick, the transistor will perform with inferior confinement effect for holes. Then, the charge storage in neutral-emitter region will enhance the base recombination current and increase the total base current. In other words, though a relatively low offset voltage could be achieved, the current gain might be decreased particularly under large forward B–E bias [6]. On the other hand, if a thinner as well as small energy-gap emitter layer is employed, the device will serve as conventional HBTs and the undesirable offset voltage is still considerably large.

The second approach to improve the turn-on voltage is to adopt small energy-gap InGaAs or GaAsSb ternary alloys as base layer, however, they introduces compressive strain and the base layer thickness is critical due to a lattice mismatch with GaAs material [8,9]. In addition, the use of the $In_xGa_{1-x}As_{1-y}N_y$ as base layer have been demonstrated to further reduce the energy-gap of base and it effectively improved the problem associated with excess strain [10]. Unfortunately, the blocking effect of collector current at base–collector heterojunction could induce a large knee voltage and reduce the collector current.

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0038-1101/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2008.02.006

In this paper, InGaP/GaAs heterostructure-emitter bipolar transistors (HEBTs) with InGaAs/GaAs superlattice and quantum-well base structures are demonstrated and compared. Similar to the conventional HEBTs, the addition of a thinner as well as small energy-gap emitter layer helps to eliminate the potential spike at B–E junction. Significantly, the average energy-gap in the base region is decreased by the use of the superlattice or quantum-well base structures. The influence of superlattice and quantum-well bases on the device characteristics will be illustrated.

2. Device structures

The device structure of the superlattice-base device (labeled device A) consists of a 0.5 μm $n^+ = 1 \times 10^{19}$ cm^{-3} GaAs subcollector layer, a 0.5 μm $n^- = 5 \times 10^{16}$ cm^{-3} GaAs collector layer, a $p^+ = 5 \times 10^{18}$ cm^{-3} InGaAs/GaAs superlattice-base, a 300 Å $n = 5 \times 10^{17}$ cm^{-3} GaAs emitter layer, a 0.1 μm $n = 5 \times 10^{17}$ cm^{-3} $In_{0.49}Ga_{0.51}$ P confinement layer, and a 0.3 μm $n^+ = 1 \times 10^{19}$ cm^{-3} GaAs cap layer. The superlattice-base consists of ten-period 50 Å $In_{0.2}Ga_{0.8}As$ layers and nine-period 50 Å GaAs layers. As to the quantum-well base device (labeled device B), its structure is similar to the device A except that a 50 Å $p^+ = 5 \times 10^{18}$ cm^{-3} $In_{0.2}Ga_{0.8}As$ quantum-well and a 900 Å $p^+ = 5 \times 10^{18}$ cm^{-3} GaAs base layer are employed to replace the superlattice-base. For comparison, the conventional InGaP/GaAs HEBT (labeled device C) with a 950 Å $p^+ = 5 \times 10^{18}$ cm^{-3} GaAs material is used as base bulk layer. The concentration and the total thickness in the base region of the three devices are estimated as the same. In general, as the base layer is made with InGaAs bulk material, the thickness of the InGaAs layer is severely limited due to the high strain resulting from the lattice mismatch [8]. Previously, the electronic and photonic properties of InGaAs/GaAs long-period superlattices have been demonstrated because the strain of the superlattices could be released [11–13]. Thus, the thickness of the studied device with the superlattice-base is applicable. A two-dimensional (2D) semiconductor simulation package SILVACO was employed to analyze the energy-band diagrams, distributions of electrons and holes, and dc performance of the devices [14]. The two-dimensional analysis takes into account the Poisson equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously. In the three devices, the emitter and collector areas are 50×50 and 100×100 μm^2, respectively.

3. Result and discussion

In the studied devices, a 300 Å n-GaAs emitter layer inserted between confinement and base layers enables the pn junction to act as a homojunction, and its thickness is sufficient to lower the energy-band at emitter side for eliminating the potential spike. Fig. 1(a)–(c) illustrate the energy-band diagrams near the B–E junction for the devices A–C, respectively. Obviously, the potential spikes at B–E junction of all devices are entirely eliminated, even at $V_{EB} = 1.0$ V.

Fig. 2 shows the simulated common-emitter current–voltage (I–V) characteristics of the three devices at room temperature. Clearly, the device A (superlattice-base device) exhibits a highest collector current and a largest current gain, while the device B (quantum-

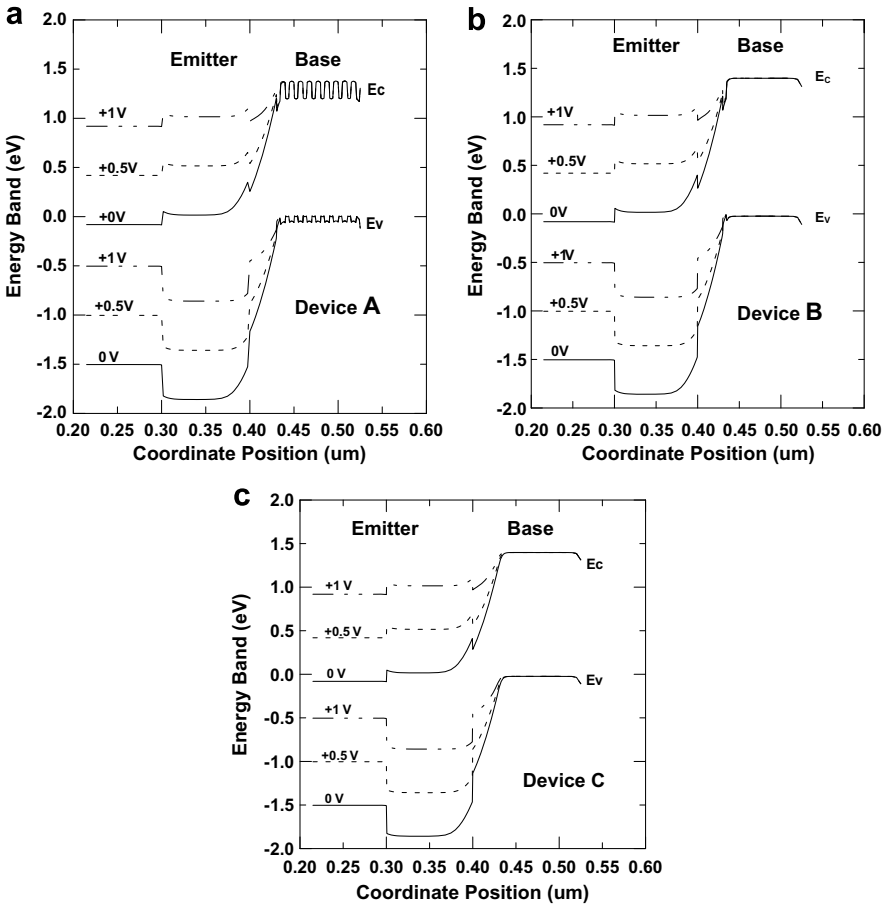

Fig. 1. Energy-band diagrams near the base–emitter junction of (a) device A (superlattice-base HEBT), (b) device B (quantum-well base HEBT), and (c) device C (traditional HEBT). The solid and dashed lines represent the diagrams at equilibrium and under base–emitter forward biases, respectively.