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In-depth electrical characterization of sub-45 nm fully depleted strained SOI MOSFETs with TiN/HfO_2 gate stack

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Abstract

We investigate the performance of strained silicon directly on insulator for short and narrow fully depleted strained silicon on insulator (FD-sSOI) CMOS transistors with a TiN/HfO_2 gate stack in two different orientations. Through electrical characterization of these devices versus the geometry and for different wafers (with different strain levels), a mobility enhancement and low short and narrow channel effects are put in evidence. Moreover, elastic mechanical simulations, based on Hooke's law, are performed in order to understand the carriers' sensitivity to strain and to MESA induced stress relaxation. Finally, a specific method of channel separation is presented in order to find both the lateral and the front contributions on the carrier transport properties of these c-MOSFETs.

Keywords: c-MOSFET; FD-SOI; Strain; SCE; NCE; Low field mobility; TiN/HfO_2 gate stack

1. Introduction

Improving the carrier mobility is highly required by the International Technology Roadmap for Semiconductor (ITRS) for the MOSFET downscaling [1]. However, with the continuous miniaturization of CMOS technologies, it becomes more and more difficult to integrate stressors, such as contact etch stop layer (CESL), between the gate and the contact area for a local strain (i.e. process induced strain) [2]. Thus, global strain using strained FD-SOI becomes a relevant alternative for any mobility improvement as well as better short channel effects (SCE) and narrow channel effects (NCE) control [3–7]. Previous studies showed that the global strain tends to relax in narrow sSOI lines [4,6,7]. In this work, FD-sSOI CMOS transistors [8], with very aggressive dimensions for both gate length and width and also for two different devices orientations, are analysed in details and they showed excellent electrical performances. We investigate mainly the impact of strain amount on SCE, NCE as well as on the stress-induced mobility gain down to 25 nm gate length and width.

This paper is organized in four sections. Following the introduction, Section 2 describes the experimental details of this study. Then, Section 3 presents the main results and the extracted parameters. Finally, in the last section, we will conclude.

2. Experimental details

Standard (001) SOI and sSOI substrates (both with 145 nm buried oxide) from SOITEC have been used in this study. The integration process has been done at the CEA-LETI. The sSOI substrates have been processed using a relaxed $Si_{0.8}Ge_{0.2}$ or $Si_{0.7}Ge_{0.3}$ starting layers [7,8]. Both types of wafers have been thinned down to 9 nm by sacrificial oxidations. The final biaxial tensile stress has been estimated around 1.3 and 1.9 GPa by Raman measurement [9], respectively. Minimum gate lengths and widths, obtained by e-beam lithography, are both 25 nm. After

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the active area patterning and etching (MESA isolation), 3 nm MOCVD HfO_2 + 10 nm PVD TiN + 50 nm polysilicon layers have been deposited to build the gate stack. After the gate etching, a 10 nm thick nitride spacer has been fabricated prior to the HfO_2 etch. The final equivalent oxyde thickness (EOT) is estimated around 1.7 nm from C–V measurement. A 2-step selective epitaxy process has been adopted in order to reduce the access resistance. The first epitaxy has been carried out just after the HfO_2 etch process and before the LDD implantation, reducing the LDD region resistance. The second one has been performed after the second spacer processing and before the source/drain implantation. NiSi has then been used, followed by a standard BEOL process. The silicon channel has been kept non-intentionally doped.

Fig. 1 presents the transmission electron microscopy (TEM) cross-section of a 30 nm wide FD-sSOI transistor with the surrounding TiN/HfO_2 gate stack. The test structures were CMOS transistors with variable gate length and variable gate width ranging from 25 nm to 10 μm. The main devices orientation is in ⟨1 1 0⟩ direction. However, the effect of the ⟨1 0 0⟩ direction is also studied.

Static I–V and C–V measurements have been performed at wafer level with a SussMicroTec LT probe station at ambient temperature (i.e. 300 K) and in dark room conditions. I–V characteristics were recorded with an HP 4155 semiconductor analyzer. C–V measurements were performed with an HP 4284 LCR meter. In order to minimize interferences, the Device Under Test (DUT) is enclosed in a Faraday cage.

The MOSFET parameters were mainly extracted using the Y-function method. It is defined as the ratio between the drain current I_d and the transconductance g_m square root. For NMOS transistors operated in linear region (i.e. small drain voltage, typically V_d equals to some 10 mV for NMOS) and at strong inversion regime, it is expressed by [10]

$$Y(V_g) = I_d/\sqrt{g_m} = \sqrt{G_m \cdot V_d} \cdot (V_g - V_{tCH}), \quad (1)$$

where I_d is the drain current in linear regime; g_m corresponds to the transconductance; V_d and V_g are the drain-to-source and gate-to-source voltages, respectively; V_{tCH} is the device charge threshold voltage; $G_m = C_{ox}\mu_0 W/L$ is the transconductance parameter with μ_0 being the low field mobility; C_{ox} denotes the maximum gate to channel capacitance (around 1.45 μF cm^{-2}); W and L represent the electrical channel width and length, respectively. W and L have been estimated by TEM and inferred by capacitance measurements. Note that a trimming of 15 nm is taken into account for L.

The linear part of the $Y(V_g)$ curves, at strong inversion, enables the extraction of μ_0 and V_{tCH} from slope and intercept, respectively. Note that one of the main advantages of this extraction method is that it is independent of the source–drain series resistance (R_{SD}) effect and of the first order mobility attenuation factor (θ_1) [10]. However, it is well known that this extraction can be difficult in modern devices mainly due to uncertainties in the effective gate length and width of short and narrow channel devices. Then, the obtained values can be disturbed, which leads to a light dispersion of the results.

In order to extract the different key parameters of n-MOSFETs (p-MOSFETs), we apply to the DUT a source voltage bias to the ground $V_s = 0$ V (the source is common to all transistors), the drain voltage bias V_d equals to 10 mV (−10 mV) and 20 mV (−20 mV) and the voltage bias V_g varies between 0 V (−1.5 V) and 1.5 V (0 V) by step of 50 mV (−50 mV). Note that the bulk is connected to the ground through the chuck (i.e. $V_b = 0$ V).

3. Results and discussion

The control of threshold voltage as well as mobility is a key issue for deep-submicronic MOSFETs. In this section, we report the results of a detailed investigation of these parameters for NMOS and PMOS transistors realised from two processes-induced strain (sSOI) and a reference SOI wafer in function of both channel length and channel width for two different orientations ⟨1 1 0⟩ and ⟨1 0 0⟩.

3.1. SCE and NCE effects

Typical I_d–V_g transfer characteristics of CMOS transistors illustrating the SCE and NCE effects are shown in

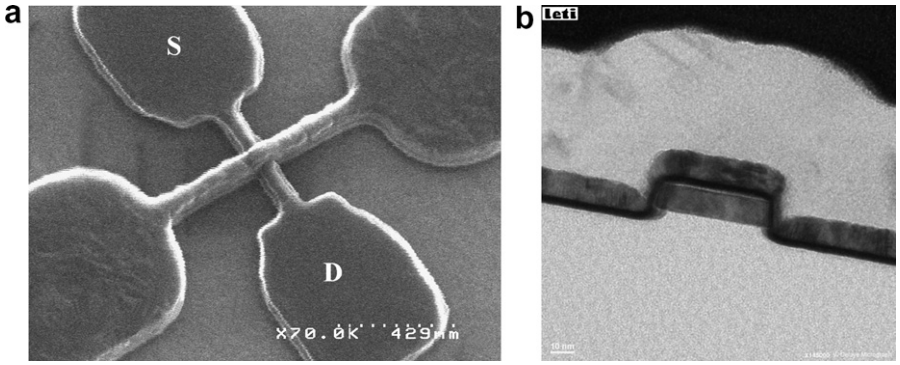

Fig. 1. (a) Top-down view of a device under test and (b) TEM cross-section of a FD-sSOI transistor in the width direction.