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Latch-up effects in CMOS inverters due to high power pulsed electromagnetic interference

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ABSTRACT

Latch-up effects in two stage cascaded CMOS digital inverters due to high power pulsed electromagnetic interference, are reported. Latch-up was observed to occur at and above 25.5 dB m of pulsed interference at frequencies of 1.23 GHz and 4 GHz. When a latch-up event occurred, the devices failed to respond to the input logic signal even after the pulsed interference was removed. Devices required to be reset to return to normal operation. Latch-up for pulsed interference at the higher frequency of 4 GHz occurred at higher power levels, indicating a suppression of the interference effects at higher frequencies due to the by-pass path effects provided by the intrinsic device capacitances. High power interference induced excess carriers and the corresponding body currents that activated the parasitic bipolar transistor action were found to play a key role in triggering the latch-ups, and are proposed here as the main mechanism for the upsets. The parasitic resistances R1 and R2 for the cascaded inverters were calculated to be 4.3 and 2.8 kΩ, respectively, and the corresponding excess body currents triggering the latch-ups were 0.163 and 0.25 mA, respectively.

1. Introduction

Electromagnetic interference from high power microwave (HPM) sources can cause serious upsets in integrated circuits (IC's) and systems [1–3]. The critical upsets in static and dynamic operation and catastrophic physical failures in MOSFET devices and CMOS digital inverters under high power continuous wave (CW) interference have been reported in [4–8]. High power pulsed electromagnetic interference is also expected to cause serious upsets and failures. Higher susceptibility of electronic systems to pulsed high power microwave and ultra wide band (UWB) sources has been reported to occur most prominently in the L (1.3 GHz) and S (2.857 GHz) bands and depended on pulse characteristics such as pulse repetition rate, pulse and burst length, and pulse duration [2]. The reported effects suggested susceptibility and failure at the electronic component level [2]. In the case of digital logic integrated circuits upset mechanisms and their relation to pulsed interference characteristics at the fundamental electronic component level such as the CMOS inverters, are still not fully understood.

One of the failure mechanisms in CMOS digital ICs is that of latch-up. Latch-ups in CMOS devices can occur when the parasitic bipolar transistor action in the body is triggered, thus enabling conduction through the body rather than through the intended operational n and p-channels of the MOSFET devices in the logic inverters, rendering the devices inoperable. Latch-ups have been reported to be triggered by overshoot and undershoot voltage spikes at outputs and inputs when the inputs are connected with electrostatic discharge (ESD) protection diodes, avalanche breakdown at the n-well junction, punch through between n-well and n+ contact, and punch through between p-substrate and p+ contact [9,10]. Latch-ups due to high power pulsed electromagnetic interference have not yet been reported.

In this work, latch-up effects in cascaded CMOS digital inverters due to high power pulsed electromagnetic interference are reported for the first time.

2. Experimental details

Two stage cascaded inverters, consisting of two identical CMOS inverters with a width to length ratio (W/L) of 3.2 μm/1.6 μm for the n-channel MOSFETs, and 9.6 μm/1.6 μm for the p-channel MOSFETs, were designed and fabricated into packaged chips. The chips were placed on an RT Duroid 5880 board designed for microwave measurements under matched 50 Ω conditions. Prior to any measurements under pulsed EMI, the reflection of the interference

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signal was monitored to be less than 3% of the transmitted signal. However, for simplicity, the nominal applied power is quoted in these experiments. The output voltage of the first stage inverter (V_{O1}) was measured using a Tektronix TDS 540 C digital oscilloscope as pulsed electromagnetic interference (PEMI) signal was injected into the input of the cascaded inverters through a bias-T, as shown in Fig. 1. For the pulsed interference signal a continuous wave (CW) signal was generated using a HP E4438 C signal generator, pulsed by providing an external trigger from a Standford Research System pulse generator, and then amplified through an Ophir RF amplifier. The peak power of pulsed interference signal ranged from 0 to 33 dB m and the frequency was 1.23 GHz and 4 GHz. The width and period of the pulse signal were 800 ns and 10 ms, respectively.

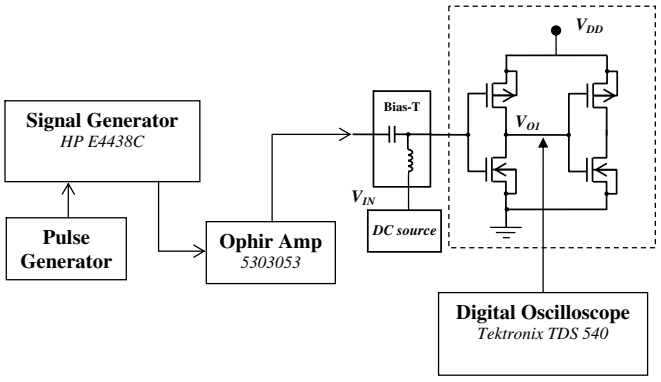

Fig. 1. Schematic of the measurement set-up. The output voltage (V_{O1}) of the first stage inverter in the cascaded inverters was measured using a digital oscilloscope.

3. Latch-up effects under pulsed EMI

The effects of pulsed EMI on the output voltage of the cascaded inverters is examined in this section. The output voltage (V_{O1}) of the first stage inverter in the cascaded inverters with input logic low (V_{IN} = 0 V) was measured under 1.23 GHz pulsed interference. The width and period of the pulsed interference was 800 ns and 10 ms, respectively. The output voltage without interference (V_{O1} = 5 V) decreased to lower voltage when the pulse was ON, indicating bit errors, as shown in Fig. 2. The reduction in V_{O1} increased gradually with increasing interference power, but returned to normal condition (5 V) when the pulse was OFF for interference power levels up to 25.5 dB m (Fig. 2b), indicating a soft reversible error. At the pulse power level of 25.5 dB m the output voltage (V_{O1}) showed a gradual decrease to 1.7 V (Fig. 2b). At the 25.5 dB m power level repeated pulses resulted in a bit error at first, and then in latch-up to 1.23 V with further pulses (3 s total

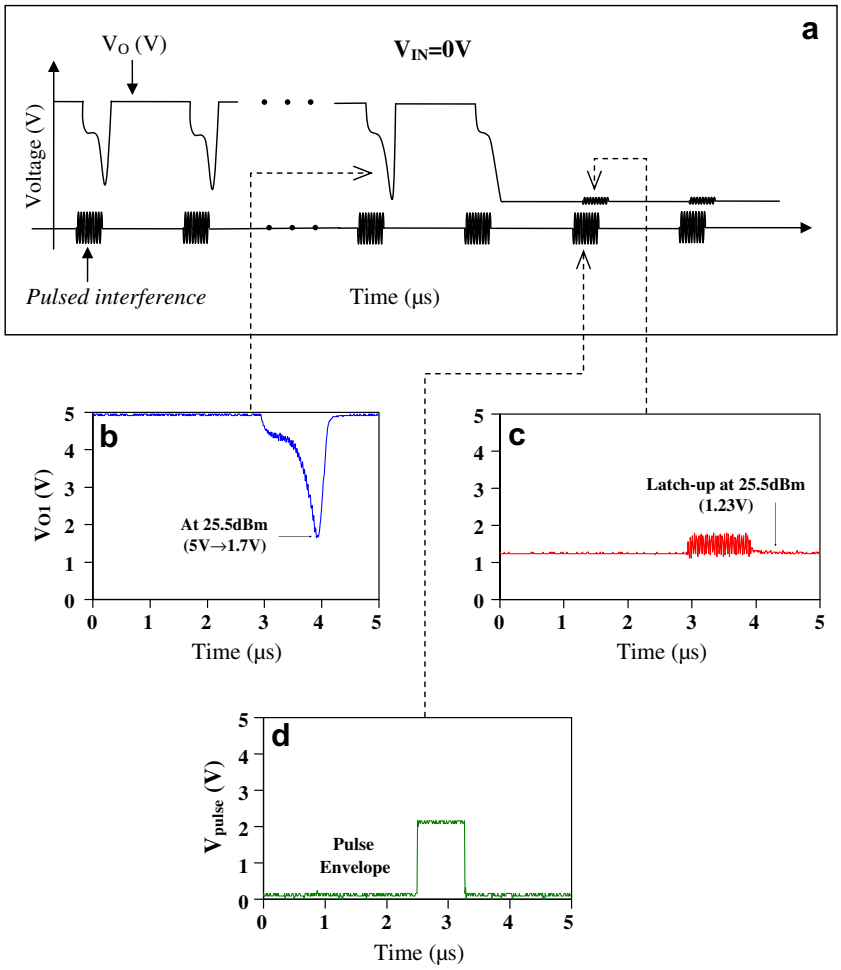

Fig. 2. Measured output voltage (V_{O1}) of the first inverter for input logic low (V_{IN} = 0 V) under pulsed EMI signal at 1.23 GHz. The width and period of the pulses were 800 ns and 10 ms, respectively. (a) Total schematic representation of V_{O1} and the pulsed interference. (b) Measured output voltage showing a bit error from 5 V to 1.7 V at 25.5 dB m. (c) Measured output voltage showing latch-up to 1.23 V at 25.5 dB m after repeated pulses. The device failed to respond even after the pulsed interference was removed. The device gained normal operation only after resetting the power supply (V_{DD}). (d) The actual measured envelope of the pulsed interference signal.