Solid-State Electronics 52 (2008) 1610–1614

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Gate dielectric engineering of quarter sub micron AlGaN/GaN MISHFET: A new device architecture for improved transconductance and high cut-off frequency

Ruchika Aggarwal [a], Anju Agrawal [b], Mridula Gupta [a], R.S. Gupta [a,*]

[a] Semiconductor Devices Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi 110021, India
[b] Department of Electronics, Acharya Narendra Dev College, University of Delhi, Kalkaji, New Delhi 110019, India

ARTICLE INFO

Article history:
Received 15 May 2008
Accepted 7 June 2008
Available online 22 July 2008

Review of this manuscript was arranged by A. Iliadis, C. Richter, and A. Zaslavsky

Keywords:
AlGaN/GaN MISHFET
Cut-off frequency
Gate dielectric engineering
T-gate
Γ-gate
Transconductance
Transconductance generation efficiency

ABSTRACT

In this paper analytical modeling for a novel three region gate dielectric engineered AlGaN/GaN Metal Insulator Semiconductor heterostructure field effect transistor (MISHFET) device architecture is presented which shows high transconductance and enhanced cut-off frequency at quarter micron gate lengths. Using a three region analysis along the horizontal direction in the gate dielectric region the expressions for transconductance and cut-off frequency of the device are obtained. It has been observed that using these gate dielectric schemes, improvements on device performance are observed over conventional MISHFET structures. Relative comparison of T and Γ-gate shaped structures is done with uniform gate dielectric profile and enhancement in microwave performance is observed. The proposed model is capable of modeling electrical characteristics like drain current, output conductance and threshold voltage of various other existent structures like uniform gate dielectric MISHFETs, HFETs and T-gate HFETs. The present model is based on closed form expression and does not involve any fitting parameter. The results obtained are compared with experimental data and show excellent agreement, thereby proving the validity of the model.

© 2008 Elsevier Ltd. All rights reserved.

1. Introduction

The gallium nitride (GaN) and its related alloys based semiconductor materials have been attracting attention because of their large bandgap and their ability to operate at high power, high temperature and high speed. Such qualities have led to investigation of these material systems for various devices including metal insulator semiconductor heterostructure field effect transistors (MISHFETs), HFETs, heterojunction bipolar transistors (HBTs), metal oxide semiconductor field effect transistors (MOSFETs), photodiodes and photodetectors. Tremendous commercial applications await any successful and desirable demonstration of these devices. Radio frequency (RF) power amplification is one example where AlGaN/GaN HFETs are sought after [1,2]. However, large gate leakage currents and inferior noise characteristics of AlGaN/GaN HFETs led to the development of AlGaN/GaN based MISHFET structure. The AlGaN/GaN MISHFET is characterized by a thin gate dielectric and has received much attention recently due to its capability to combine the advantages of dielectric layer and AlGaN/GaN heterostructure. The MISHFET approach allows for application of high positive gate voltages to further increase the sheet carrier density in the 2-DEG channel and hence the device peak currents [3–6]. It has demonstrated excellent electrical performance and applications such as high frequency wireless base stations, broad band links, etc. Commercial and military radar and satellite communication could benefit from such a device. However, there are many milestones to be achieved and the work in this field is far from complete. In order to achieve superior RF performance for high frequency applications, short gate length is required for compound field effect transistors. The gain and noise characteristics of the MISHFETs at high frequency are strongly dependent on the gate length and the gate resistance values. Several gate dielectric engineered structures like T-gate, Γ-gate [7] etc. are currently being used for reliability improvement for low noise and high gain characteristics. T-shaped gate structures are most extensively studied as they are characterized by small foot which defines the small gate length and the wide top which provides a low gate resistance [8]. Different lithography methods have been developed for the submicrometer T-gates in recent years [9,10]. For example, multilayer photo resist processes have been used to obtain submicrometer T-shaped gates [11]. In order to further improve device performance, dielectric deposition process with etching back technology have been widely used to form dielectric sidewall and shrink the gate length that is originally limited by the lithography resolution [12]. The thermally reflowed resist process is another approach for gate shrinkage and has been reported by Meng and

* Corresponding author. Tel.: +91 11 2411 5580; fax: +91 11 2411 0606.
E-mail addresses: ruchikaaggarwal83@yahoo.co.in (R. Aggarwal), rsgu@bol.net.in (R.S. Gupta).

0038-1101/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2008.06.008

Lee et al [13–14]. Tightly controlled process and relatively complicated steps are required for these processes. However, challenges posed by fundamental limits have led to the continuous exploration of new device structures for the technological progress of semiconductor industry. Therefore to utilize the combined advantages of both T-shaped structure and AlGaN/GaN MISHFET, we for the first time have theoretically proposed the gate dielectric engineering for AlGaN/GaN MISHFET structure and systematically examined its effect on electrical characteristics of the proposed device. Different combinations of dielectrics like SiO_2, Si_3N_4 have been investigated. A closed form expression for drain current has been formulated by taking into account the highly dominant effect of spontaneous and piezoelectric polarization at the AlGaN/GaN interface. The proposed model includes E_f as a function of n_s by a simple polynomial in the $n_s - V_{gs}$ expression and account for the whole range of operation i.e. from subthreshold to deep saturation region. The proposed analysis can also predict the performance of HFETs by adjusting few parameters. The effects of parasitic source drain resistances and velocity saturation have also been included to accurately develop the dc model. To generalize the model, the pulse doped structure comprising the Schottky cap layer, dopant layer and spacer layer is employed. Other relevant parameters like threshold voltage, 2-DEG (two dimensional electron gas) density, transconductance and cut-off frequency have also been examined. Results are validated by available experimental data [6]. The new gate engineered MISHFET exhibits high transconductance and improved cut-off frequency.

2. Model formulation

The basic schematic structure used in the analysis alongwith proposed gate dielectric schemes is shown in Fig. 1. It consists of SiC substrate, an undoped GaN layer to form 2-DEG channel, an undoped AlGaN spacer layer of thickness d_i, a n-doped AlGaN layer of thickness d_d to provide 2–DEG and an undoped AlGaN cap layer of thickness d_s. To study the effect of position of dielectric and their thicknesses, the region between gate and the high band gap semiconductor viz. AlGaN is divided into three identical rectangular regions. Poisson's equation is then solved separately for each identical rectangular region to maintain the continuity of current flow amongst the three regions. Each region has dimensions $L_g/3 \times t_{in}$ where L_g is the normal gate length and t_{in} is the thickness of the dielectric and is characterized by electric permittivity ε_{inz} where $z = 1, 2, 3$ for regions I, II and III, respectively. These three rectangular structures are then analyzed for different combinations of two different dielectrics viz. Si_3N_4 and SiO_2 as given in Table 1. These gate dielectric schemes are then broadly categorized into T and Γ shaped schemes based on performance resemblance to T and Γ gate HFET structures. They are then compared with the uniform schemes for both dielectrics. For current conduction through the device, the current should flow through all the three regions consistently. Hence the actual threshold voltage of the device is determined by the lowest threshold voltage amongst the three regions. The electrical characteristics of scheme A are similar to schemes B and C. Analogous is the case for scheme D with schemes E and F. The expression for 2-DEG sheet carrier density is calculated region-wise as in [15,18] and is as follows:

Table 1
Region-wise distribution of gate dielectric permittivities

Label	Region I	Region II	Region III	Gate dielectric scheme
A	SiO_2	Si_3N_4	SiO_2	T-shape
B	Si_3N_4	SiO_2	SiO_2	
C	SiO_2	SiO_2	Si_3N_4	
D	Si_3N_4	Si_3N_4	SiO_2	Γ-shape
E	SiO_2	Si_3N_4	Si_3N_4	
F	Si_3N_4	SiO_2	Si_3N_4	
G	Si_3N_4	Si_3N_4	Si_3N_4	Uniform Si_3N_4
H	SiO_2	SiO_2	SiO_2	Uniform SiO_2

$$n_{sz}(x) = \frac{\beta}{q(d_t + \alpha)}[V_{geff} - V_{thz} - E_f] \tag{1}$$

And respective threshold voltage for each region can be expressed as:

$$V_{thz} = \phi_b(m) - \Delta E_c - \frac{qN_d d_d^2}{2\beta}\left(1 + \frac{2d_s}{d_d}\right) - \frac{qN_d t_{in} d_d}{\varepsilon_o \varepsilon_{inz}} - \frac{\sigma_{pz}(m)(d_t + \alpha)}{\beta} + k_1 \tag{2}$$

where $\alpha = \frac{\varepsilon_s t_{in}}{\varepsilon_{inz}}$, $\beta = \varepsilon_0 \varepsilon_s$, $V_{geff} = V_{gs} - V(x)$ is the effective gate voltage and $V(x)$ is the channel potential at any point x due to the drain voltage, V_{gs} is the applied gate voltage, $\phi_b(m)$ is the Schottky barrier height between bulk semiconductor and gate electrode, ΔE_c is the conduction band discontinuity, N_d is the doping concentration of

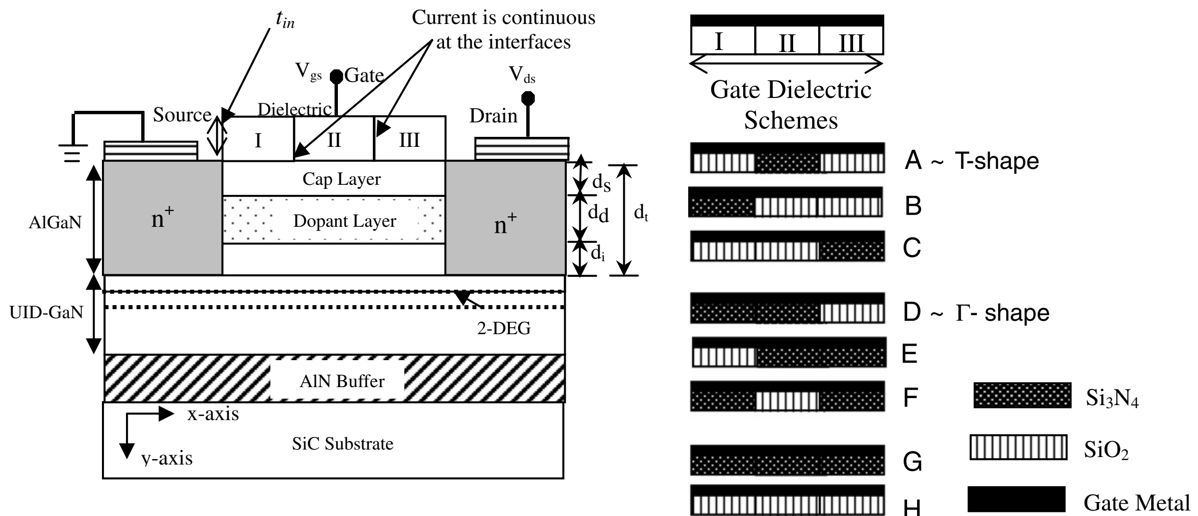

Fig. 1. Cross-sectional view of gate dielectric engineered AlGaN/GaN MISHFET alongwith various gate dielectric schemes.

Download English Version:

https://daneshyari.com/en/article/749194

Download Persian Version:

https://daneshyari.com/article/749194

Daneshyari.com