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Self-aligned inversion n-channel $In_{0.2}Ga_{0.8}As$/GaAs metal–oxide–semiconductor field-effect-transistors with TiN gate and $Ga_2O_3(Gd_2O_3)$ dielectric

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ABSTRACT

A self-aligned process for fabricating inversion n-channel metal–oxide–semiconductor field-effect-transistors (MOSFET's) of strained $In_{0.2}Ga_{0.8}As$ on GaAs using TiN as gate metal and $Ga_2O_3(Gd_2O_3)$ as high κ gate dielectric has been developed. A MOSFET with a 4 μm gate length and a 100 μm gate width exhibits a drain current of 1.5 mA/mm at $V_g = 4$ V and $V_d = 2$ V, a low gate leakage of $<10^{-7}$ A/cm^2 at 1 MV/cm, an extrinsic transconductance of 1.7 mS/mm at $V_g = 3$ V, $V_d = 2$ V, and an on/off ratio of $\sim 10^5$ in drain current. For comparison, a TiN/$Ga_2O_3(Gd_2O_3)$/$In_{0.2}Ga_{0.8}As$ MOS diode after rapid thermal annealing (RTA) to high temperatures of 750 °C exhibits excellent electrical and structural performances: a low leakage current density of 10^{-8}–10^{-9} A/cm^2, well-behaved capacitance–voltage (C–V) characteristics giving a high dielectric constant of ~16 and a low interfacial density of state of $\sim(2\sim6) \times 10^{11}$ cm^{-2} eV^{-1}, and an atomically sharp smooth $Ga_2O_3(Gd_2O_3)$/$In_{0.2}Ga_{0.8}As$ interface.

1. Introduction

Alternative high κ gate dielectrics (replacing conventional SiO_2) and metal gates have been implemented on the 45 nm node microprocessors resulted from the extensive research efforts in the past decade due to the aggressive scaling of Si complementary metal oxide semiconductors (CMOS). For the 22 nm node technology and beyond, Si channel may have to be replaced with semiconductors of higher carrier mobility. Feverish research activities are now being taken on high κ dielectrics on high-mobility channel materials, such as GaAs and its related III–V compound semiconductors.

Ultra-high vacuum (UHV) deposited $Ga_2O_3(Gd_2O_3)$ (GGO) [1–4] and atomic layer deposited (ALD) Al_2O_3 [5–9] and HfO_2 [10,11] on GaAs and InGaAs have unpinned the surface Fermi level of oxide/III–V hetero-structures without any interfacial layers. Furthermore, low interfacial densities of states (D_{it}'s), low electrical leakage current densities, high temperature thermodynamic stability of the hetero-structures, and smoothness and abruptness of the oxide/III–V interface in an atomic scale after high temperature annealing, critical for the III–V MOSFET's, have been achieved. The first inversion n- and p-channel GaAs MOSFETs have been demonstrated using GGO as the gate dielectric and a non-self-aligned process [12,13].

In this work, a self-aligned gate process for fabricating inversion n-channel MOSFET's of strained $In_{0.2}Ga_{0.8}As$ (InGaAs) on GaAs using TiN as the gate metal and GGO as the gate dielectric has been developed. For comparison, a TiN/GGO/InGaAs MOS diode was tested with rapid thermal annealing (RTA) and has shown excellent electrical and structural characteristics, as studied using capacitance–voltage (C–V) and current–voltage (I–V) measurement, and high-resolution transmission electron microscopy (HR-TEM).

2. Experimental

A cross-sectional schematic of the n-channel InGaAs MOSFET is shown in Fig. 1. A p-well, consisting of an $In_{0.2}Ga_{0.8}As$ (7~8 nm thick) strained-epilayer with a Be doping of 5×10^{16} cm^{-3} on GaAs (300 nm thick) with the same p-doping, was grown on 2-in. semi-insulating GaAs substrates using solid-source GaAs-based molecular beam epitaxy (MBE). After the epilayer growth, e-beam evaporated $Ga_2O_3(Gd_2O_3)$ of various thickness was deposited *in situ* on the InGaAs layer. The detailed procedure on the oxide growth carried out in a multi-chamber MBE system was given earlier [1–4].

The device fabrication using a self-aligned process started with a gate region definition using a lift-off process. TiN as the gate metal was formed by reactive sputtering from a pure Ti target in Ar/N_2

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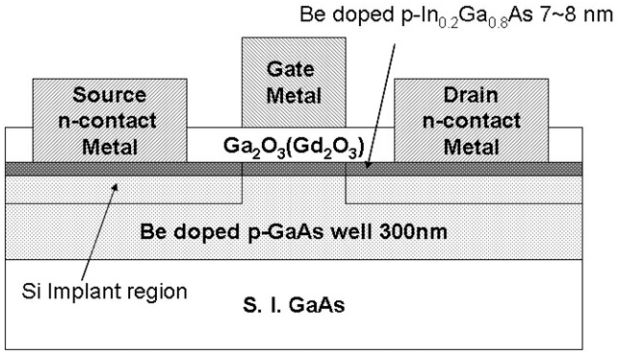

Fig. 1. Schematic cross-section of MOSFET device structure.

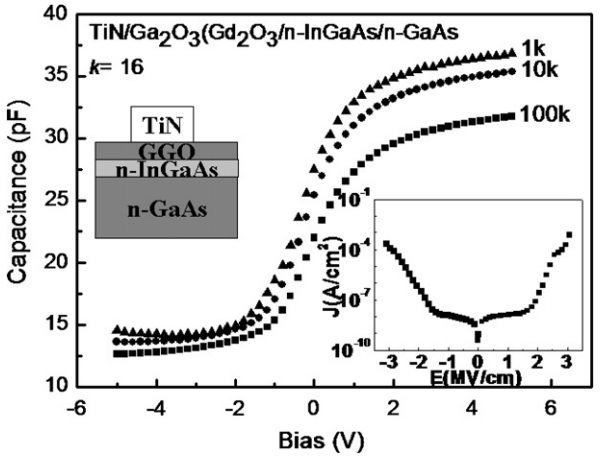

Fig. 2. *C–V* curve of TiN/$Ga_2O_3(Gd_2O_3)$/n-$In_{0.2}Ga_{0.8}As$/n-GaAs MOS diode after RTA to 750 °C(dwell for 30 s) under N_2 measured under 1, 10, 100 kHz. The corresponding *J–E* curve is shown in inset.

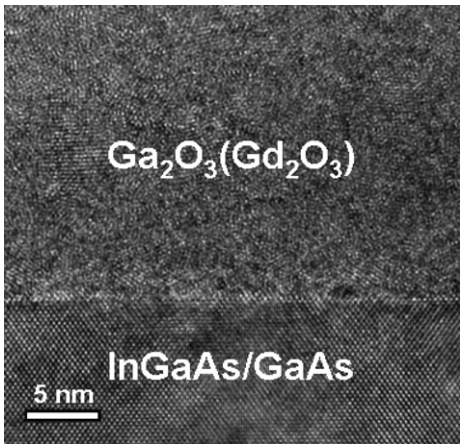

Fig. 3. Cross-sectional HR-TEM micrograph of the sample from Fig. 2 showing atomically smooth and abrupt interface of $Ga_2O_3(Gd_2O_3)$/n-InGaAs/n-GaAs.

RF-plasma. Si was used as the n-type dopant for Ohmic contact in source/drain (*S*/*D*) region for the n-MOSFET. A photo-resist and the gate metal were both used to define the *S*/*D* region during the implantation. A high temperature annealing, critical for activating the implanted dopant, has been tailored to preserve the smoothness of the metal/oxide and oxide/semiconductor interfaces at an atomic level. An intermediate temperature (375) annealing was performed prior to rapid thermal annealing (RTA) to 750 °C (dwelling for 30 s) under pure N_2 gas. [14,15] Moisture absorbed during air exposure was driven out during the 375 °C annealing, thus ensuring the thermodynamic stability of GGO/InGaAs during the high temperature activation anneal. A dilute HCl solution was used to remove GGO [16] in the *S*/*D* region prior to the metal deposition. Ohmic contact alloying was performed at 400 °C for 1 min in helium gas. Finally, the pads for measurement were deposited using e-beam evaporated Ti/Pt (30 nm/70 nm) metal stacks.

The MOS diode samples were prepared on GaAs N^+-substrates in a procedure similar to what was described for the MOSFET, with the p-well replaced by epi-layers of Si-doping of 4×10^{17} cm^{-3}. The N^+-substrates were chosen simply for easy formation of ohmic contacts on the backside of the substrates. The gate metal and heat treatments for the MOS diodes were the same as those for the MOSFET devices.

The device electrical characteristics of the MOSFET were measured using Agilent 4156 C. $J - E_G$ (current density versus electrical field) and *C–V* (capacitance versus voltage) characteristics were measured using Agilent 4156 C and 4284, respectively. HR-TEM specimens were prepared with mechanical polishing, dimpling, and ion milling using a Gatan PIPS system operated at 4 kV. HR-TEM images were taken using a field-emission microscopy (JEM-2100F) operated at 200 kV.

3. Results and discussion

The TiN/GGO/InGaAs MOS diode with RTA to 750 °C exhibits excellent performances, e.g. well-behaved *C–V* curves (Fig. 2) expected for an unpinned oxide/InGaAs interface. A dielectric constant of GGO is calculated to be about 16. Using the room temperature high frequency Terman method [17], the distribution of D_{it} (not shown here) at midgap was estimated to be $\sim(2–6) \times 10^{11}$ cm^{-2} eV^{-1}, similar to the value obtained in the as-deposited sample [14,15]. A low leakage current density of 10^{-8}–10^{-9} A/cm^2 was also achieved and shown in the inset of Fig. 2. The low leakage current reveals the high quality and robustness of the MOS structure after the high temperature annealing.

The RTA annealed TiN/GGO/InGaAs hetero-structure has revealed an atomically sharp oxide/semiconductor interface without interfacial layers, as studied using HR-TEM (Fig. 3). This smooth and sharp interface is similar to what was observed in the previously studied GGO/GaAs cases, in which gate metals were deposited after the oxide/semiconductor hetero-structures were RTA to high temperatures. [14,15,18]. The results presented here also indicate the chemical and thermodynamic stability of the TiN/GGO interface, important for the self- aligned process.

Fig. 4a shows the measured drain *I–V* curves of the self-aligned enhancement-mode inversion-channel TiN/GGO/InGaAs/GaAs NMOSFETs with a device geometry of 4×100 μm^2. The thickness of high κ gate dielectric GGO is 17 nm. The gate voltage varies from 0 to 4 V in steps of 0.5 V. The threshold voltage, V_t, is around 1.8 V and the channel inversion is clearly demonstrated. The saturation current is proportional to $(V_g - V_t)^2$ which is a typical characteristic of an enhancement-mode inversion-long-channel device. A drain current of 1.5 mA/mm is obtained at V_g of 4 V and V_d of 2 V. Fig. 4b shows the results of split-CV curve taken on a NMOSFET with 20 μm gate length and 100 μm gate width. Using split-CV method to measure the MOSFET with source and drain grounded, a clear inversion behavior in the MOS structure was observed. The drain IV characteristics in Fig 4a and the split-CV result in Fig 4b demonstrate the inversion n-channel on the TiN/GGO/InGaAs/GaAs NMOSFETs and provide the evidence of unpinned interface between GGO and InGaAs .

The gate-to-source *I–V* characteristics are shown in Fig. 5, with a small gate leakage of $<10^{-7}$ A/cm^2 at 1 MV/cm, which is similar to