Solid-State Electronics 52 (2008) 1652–1659

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Proton-induced SEU in SiGe digital logic at cryogenic temperatures

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ARTICLE INFO

Article history:
Received 30 May 2008
Accepted 7 June 2008
Available online 3 August 2008

Review of this manuscript was arranged by A. Iliadis, C. Richter, and A. Zaslavsky

Keywords:
Silicon–germanium
Radiation effects
Single event upset
Proton
Radiation hardening by design
RHBD
SEU
SiGe HBT

ABSTRACT

We present the first experimental results confirming the increased SEE sensitivity of SiGe digital bipolar logic circuits operating in a 63 MeV proton environment at cryogenic temperatures. A 3× increase in both the error-event and bit-error cross sections is observed as the circuits are cooled from 300 K to 77 K, with error signature analyses indicating corresponding increases in the average number of bits-in-error and error length over data rates ranging from 50 Mbit/s to 4 Gbit/s. Single-bit-errors dominate the proton-induced SEU response at both 300 K and 77 K, as opposed to the multiple-bit-errors seen in the heavy-ion SEU response. Temperature dependent substrate carrier lifetime measurements, when combined with calibrated 2 D DESSIS simulations, suggest that the increased transistor charge collection at low temperature is a mobility driven phenomenon. Circuit-level RHBD techniques are shown to be very efficient in mitigating the proton- induced SEU at both 300 K and 77 K over the data rates tested. These results suggest that the circuit operating temperature must be carefully considered during component qualification for SEE tolerance and indicate the need for broad-beam heavy-ion testing at low temperatures.

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1. Introduction

The electronic components employed in a wide array of space exploration applications are routinely exposed to both extreme fluctuations in temperature and a variety of energetic particles within the space radiation environment. On the surface of the Moon, for example, the ambient temperature ranges from +120 °C (393 K) during the day, to −180 °C (93 K) at night, and down to −230 °C (43 K) in shadowed polar craters [1]. The radiation environment of interest for satellite and spacecraft orbit is composed of charged particles trapped by the earth's magnetic field (*Van Allen radiation belts*); galactic, solar and terrestrial cosmic rays; solar flares; and plasma of electrons and protons extending beyond the radiation belts. Particle energies range from a few keV to GeV, with flux levels as high as 10^{12} cm^{-2} s^{-1} [2–4]. Energetic protons are known to induce degradation in semiconductor device performance via bulk displacement and ionization processes, which are typically manifested at the transistor level as FET threshold voltage shifts (ΔV_T) [5] or BJT base current leakage (ΔI_B) [6]. In addition, proton interaction with the silicon lattice via both inelastic and elastic collisions results in the creation of secondary particles which, with sufficient range and energy, can induce data upsets in logic and memory circuits [7,8]. The excess charge carriers generated as a result of the energy deposited from these interactions are efficiently collected by the strong electric fields associated with reverse bias *pn* junctions in a low resistance substrate [9]. The collected charge is subsequently coupled to sensitive circuit nodes, where they can be manifested as any number of single event phenomenon [10], including single-event upset (SEU) in silicon germanium (SiGe) digital bipolar logic, which is the focus of this work.

On-orbit event rate predictions [11] for space-based electronic systems are a vital tool for component qualification, system design, and mission planning. These rate predictions are routinely derived as the product of the orbital dependent rate coefficient and the SEU figure-of-merit, in units of upsets/bit-day [12]. The value of this rate coefficient is determined by the details of the orbit, including mission lifetime, local radiation fields, and ambient temperature. The SEU figure-of-merit is determined primarily by the heavy-ion saturation cross section (σ_{HL}) and threshold linear energy transfer (LET_0) in the case of heavy-ions; or the limiting proton cross

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0038-1101/$ - see front matter Published by Elsevier Ltd.
doi:10.1016/j.sse.2008.06.038

section (σ_{PL}) in the case of protons, as discussed in [12]. Heavy-ion broad-beam testing encompassing various ion species and incident angles is typically used to simulate a particular space environment of interest, generating the characteristic device cross section (σ) vs. linear energy transfer (LET) curve, fitted to a Weibull distribution from which the SEU figure-of-merit can be calculated. To date, such an investigation in SiGe circuits has routinely been performed at 300 K [13–15]. In this work we present, for the first time, experimental results confirming an increase in the SEU susceptibility of SiGe digital bipolar logic operating at cryogenic temperature in a 63 MeV broad-beam proton environment.

SiGe BiCMOS technology continues to mature into a key platform for extreme environment electronics applications, due to its exceptional transistor-level performance at cryogenic temperatures (f_T > 500 GHz at 5 K) [16] and built in multi-Mrad(SiO_2) total ionizing dose (TID) tolerance [17]. These attributes enable the design of key analog and RF building blocks with robust operation over a wide range of temperature and radiation specifications [18–22]. The high SEU susceptibility of bulk SiGe digital bipolar logic continues to be a major challenge, and is currently being addressed using a combination of device- and circuit-level radiation hardening by design (RHBD) techniques [23,24]. Triple modular redundancy (TMR) techniques have been successfully shown to provide sufficient immunity, at room temperature, up to LET values of 80 MeV cm^2/mg, as reported in [24]. The SEU phenomenon observed in these SiGe digital ICs in the aftermath of an ion strike is the result of drift-dominated charge collection by the strong reverse-biased electric field in the substrate to sub-collector junction. The charge collection dynamics are determined by a combination of factors, including the substrate doping, device structure and sensitive volume definition, ion angle of incidence, strike location, and ambient temperature. We investigate the effect of temperature on the SEU response of this technology using shift registers as the test platform.

2. Experiment details

2.1. Devices under test

SEU phenomena in digital SiGe bipolar logic was investigated here using 16-bit serial shift registers comprised of D-type flip-flops, input-, output- and clock-buffers, as shown in Fig. 1. These circuits were designed using a common-mode logic (CML) architecture and were fabricated in the commercially available IBM 8HP seven layer metal (7LM) SiGe BiCMOS process [25], using a heterojunction bipolar transistor (HBT) only design. The SiGe HBTs employed in the design feature peak cutoff and maximum oscillation frequencies (f_T/f_{MAX}) of 200/285 GHz, a collector to emitter breakdown voltage (BV_{CEO}) of 1.7 V, and were fabricated on an 8–10 Ω cm p-type substrate with an *in situ* doped polysilicon emitter, raised extrinsic base, and conventional 8 μm depth deep trench (DT) and shallow trench (ST) isolation. SiGe HBTs were selected with an emitter area (A_E) of 0.12×0.52 μm^2 in a single striped CBE configuration (as opposed to a multiple striped CBEBC configuration) to minimize the internal trench area [23]. The impact of circuit-level RHBD on the proton-induced SEU response was evaluated via the comparison of registers designed using either a standard master-slave (Std. M/S) flip-flop shown in Fig. 2, or a dual interleaved RHBD (DI RHBD) master-slave flip-flop shown in Fig. 3. The input and clock-buffers are identical for both register types and were designed using gated feedback cell (GFC) hardening techniques [26]. The output buffers were designed as simple ECL gates and were not hardened in any way. The circuits operate on negative ECL logic with a 0 to −300 mV peak to peak data swing, ground and −4 V supply rails and draw a tail current of 60 mA per flip-flop, for the Std. M/S based design and 130 mA per flip-flop for the DI RHBD design. From a circuit perspective, the positive feedback created by the cross-coupling of the transistors Q_{10} and Q_{11} of the storage cell in the slave latch of the standard design, shown in Fig. 2, has been shown to be the source of bit upsets following an ion strike. Limited decoupling of these transistors is achieved via replication of the pass and storage cells for each latch, as demonstrated in the dual interleaved design. In this hardened design, charge collected by any of the transistors Q_{19}, Q_{20}, Q_{21} or Q_{22} in Fig. 3 results in a reduced number of upsets compared to collection by either of the transistors Q_{10} or Q_{11} in Fig. 2. This improvement in SEU immunity has been verified using a combination of 3D DESSIS charge collection and Cadence SPICE simulations [27] and pulsed laser microprobe experiments [28].

2.2. Proton and heavy-ion testing

The 16-bit SiGe serial shift registers were irradiated in a 63 MeV proton broad-beam environment at the Crocker Nuclear Laboratory at the University of California at Davis [29,30]. This radiation

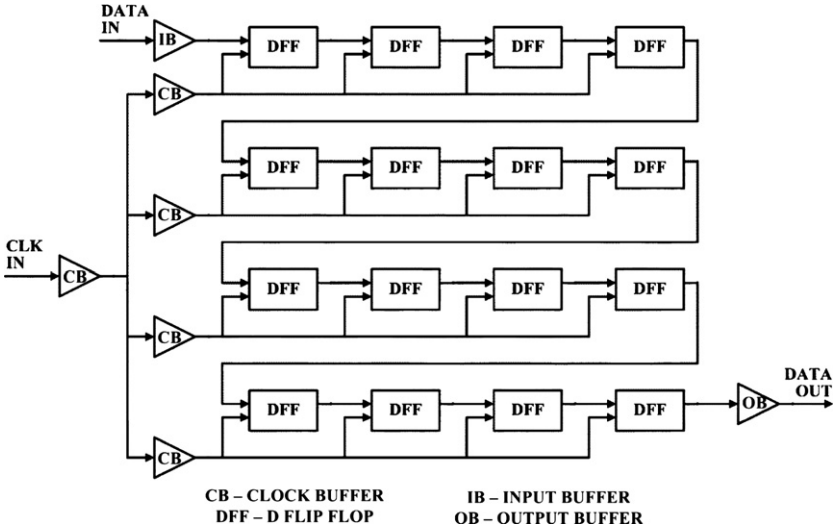

Fig. 1. Top level schematic of a 16-bit shift register showing flip-flop, clock, input, and output data buffers. Gated-feedback [26] hardening techniques are applied to the input- and clock-buffers. Registers are composed of flip-flops configured using the Std. M/S and DI RHBD D flip-flop architectures.