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Current-induced recrystallization of polycrystalline silicon nano thin films deposited at different temperatures and its influences on piezoresistive sensitivity and temperature coefficients

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ABSTRACT

To improve the performance and yield of piezoresistive sensors based on polycrystalline silicon nano thin films (PNTFs), the 80 nm-thick PNTFs were deposited on silicon (1 1 1) substrates by LPCVD at different temperatures and fabricated into cantilever beams. The electrical trimming characteristics and the dependences of gauge factor, temperature coefficient of resistance (TCR) and temperature coefficient of gauge factor (TCGF) on resistor trim with different deposition temperatures were measured. Based on the interstitial-vacancy model, the electrical trimming is explained as the mobility increase caused by current-induced recrystallization of grain boundaries. The conclusions indicate that the changes in gauge factor, TCR and TCGF with resistor trim are due to the grain boundary state variation (including scattering center, grain boundary width, tunneling current, localized and extended state conductions). And the electrical trimming method is testified to be applicable for the resistor trimming of PNTF-based sensors after packaging.

1. Introduction

As a piezoresistive material, polycrystalline silicon has many advantages over single crystal silicon, such as low cost, facile processing and no need for p–n junction isolation. Our previous research work [1,2] demonstrates that polycrystalline silicon nano thin films (PNTFs, ~80 nm in thickness) exhibit larger gauge factor ($GF \geq 34$) and better temperature stability than polycrystalline silicon thick films (more than 200 nm in thickness, GF is in the range of 20–25) at high doping levels. It makes PNTFs a potential candidate for the fabrication and application of piezoresistive sensors with low temperature drift and high sensitivity.

For sensors with Wheatstone bridge structure, the resistance accuracy and matching of bridge resistors are significant ingredients determining the zero-point output, measurement accuracy and temperature stability. However, the values of the resistors usually deviate from the design values due to the fabrication process error. Thus, it is indispensable to adjust the resistance deviation and mismatch after fabrication. The existing trimming methods include trim array [3], laser trimming [4–6], mesh laser trimming [7] and laser link making [8]. The trim array requires numerous Zener diodes or MOS transistors fabricated on a chip to adjust a single resistor, which not only wastes chip area, but also increases fabrication complexity and cost. So, this method has been adopted rarely in recent years. But the trimming methods based on laser technique have always gained considerable attentions [4–8], however, some inherent drawbacks hinder their applications. On the one hand, the utilization of laser trimmer and fabrication of peculiar resistor patterns increase equipment investment and process steps. On the other hand, the thermal stress and heat-affected zone near the kerf introduced by laser ablation can influence the long-term stability of trimmed resistors. Additionally, as a process before passivation and packaging, the laser trimming commonly increases the values of resistors and is difficult to adjust the resistance bi-directionally within the same process.

Considering the limited applicability of the above-mentioned methods, the electrical trimming for polysilicon resistors was proposed by Amemiya et al. [9] and then testified to exist in

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other polycrystalline materials [10]. After applying high current over a certain threshold to a resistor, the resistance value can decrease and then remain constant under the current lower than the threshold. The simple method has been verified to be effective and applied for the resistor trimming of some thin [11–13] and thick [14,15] films. Moreover, the trimmed resistance can increase again under suitable current [10,12]. The technique has the advantages of no damage to resistor, bi-directional trimming, low cost.

Although the electrical properties of polycrystalline silicon with electrical trimming were studied [12,13,16], the effects of the electrical trimming on its piezoresistive and temperature properties have been scarcely reported. In this paper, in order to demonstrate the feasibility of the electrical trimming for the resistor calibration of PNTF-based sensors, the electrical trimming phenomenon of heavily doped LPCVD PNTFs with different deposition temperatures and its influences on piezoresistive and temperature properties were investigated, by the measurement of film resistance, gauge factor, TCR and TCGF before and after trimming. Furthermore, the interstitial-vacancy model was established to analyze the experimental results.

2. Experimental details

2.1. Film preparation

The 80 nm-thick PNTFs were deposited by LPCVD on 500 μm-thick Si (1 1 1) substrates coated with 1 μm-thick SiO_2 layers at 580–670 °C and at 45–55 Pa. Because the 580 °C and 600 °C samples exhibited amorphous appearance with a few polycrystals, they were pre-annealed at 950 °C for 30 min to reduce amorphous contents. Then, by ion-implantation and annealing at 1080 °C for 30 min, all the samples were doped with boron and the doping concentration was estimated to be 2×10^{20} cm^{-3}.

2.2. Sample characterization

The SEM analysis was performed to characterize the surface morphology of the samples. Fig. 1(a)–(d) provides the SEM images of the samples with different deposition temperatures. In Fig. 1(a)–(d), it can be seen that the grain size increases with the increase of deposition temperature, which indicates that the crystallinity of PNTFs was improved by raising deposition temperature. Then, the XRD experiment was carried out to analyze the film microstructure and the grain orientation, and the XRD patterns are given in Fig. 1(e). The (1 1 1) peaks were attributed to the silicon substrates. For 580 °C and 600 °C samples, the weak (3 1 1) peaks were observed. For 620 °C and 670 °C samples, the (2 2 0) peaks occurred in the patterns and the intensities of the diffract peaks increased with the increase of deposition temperature. Also, the (3 3 1) peak was observed in the pattern of the 670 °C sample, testifying the improvement of film crystallinity. Noticeably, there were broad peaks (related to amorphous contents) existing in the XRD patterns (except for 620 °C samples), when $2\theta = 85–100°$. It indicates that there were less amorphous contents in 620 °C films than other samples.

2.3. Cantilever beam fabrication

Based on photolithography and wet etching, the longitudinal PNTF piezoresistors with the length–width ratio of 100 μm/400 μm were fabricated. Then, an aluminum layer was evaporated onto the samples. After patterning and alloying at 450 °C for 20 min, the contact electrodes were fabricated. By scribing the wafer, the cantilever beam samples of 26 mm × 4 mm were achieved.

2.4. Measurement of electrical trimming, piezoresistive and temperature properties

The schematic diagram of experimental setup for electrical trimming is shown in Fig. 2. Through pads and probes, the PNTF resistor was connected to the control switch, and the switch was responsible for the transformation between trimming and measuring. In the trimming step, when the terminal a and a' of the switch were connected to the terminal b and b', respectively, a constant current was applied to the PNTF resistor. The trimming time was 30 s in coincidence with [17]. In the measuring step, the terminal a and a' were switched to the terminal c and c', respectively. And the resistance value was measured by a digital multimeter. In each trimming step, the applied current amplitude was incremented gradually.

Then, the gauge factor, TCR and TCGF before and after trimming were measured utilizing the testing setup shown in Fig. 3. In the measurement of gauge factor, either end of the cantilever beam was fixed by a clamp. When an axial force F was applied to the free end of the cantilever beam, the strain $\varepsilon(x)$ produced at x could be expressed as [18]:

$$\varepsilon(x) = \frac{6(l-x)F}{bt^2Y} \tag{1}$$

where l is the force arm of the axial force F, and b and t are the width and the thickness of the cantilever beam ($b, t \ll l$ here), respectively. Y is the Young's modulus of silicon. The gauge factor was calculated by

$$\mathrm{GF} = \frac{R - R_0}{R_0\varepsilon} = \frac{\Delta R}{R_0\varepsilon} \tag{2}$$

where R_0 and R are the initial resistance without strain and the varied resistance with strain, respectively. In the experiment, the resistance values were measured by an Agilent 34401A digital multimeter.

In the measurement of temperature coefficients, the TCR is defined as

$$\mathrm{TCR}\ (\%) = \frac{\Delta R_T}{R_{ini}\,\Delta T} \times 100 \tag{3}$$

where ΔT, R_{ini} and ΔR_T are the temperature change range, the resistance at the initial temperature and the change of the resistance in the ΔT range, respectively. Similarly, the TCGF is defined as

$$\mathrm{TCGF}\ (\%) = \frac{\Delta \mathrm{GF}_T}{\mathrm{GF}_{ini}\,\Delta T} \times 100 \tag{4}$$

where GF_{ini} and $\Delta \mathrm{GF}_T$ are the gauge factor at the initial temperature and the change of the gauge factor in the ΔT range, respectively. The testing setup in Fig. 3 was placed into a constant temperature cabinet for measuring TCR and TCGF.

3. Results and discussions

3.1. Electrical trimming phenomenon and interstitial-vacancy (IV) model

The dependences of the normalized resistances of PNTF resistors on trimming current and trimming current density with different deposition temperatures are depicted in Fig. 4. It could be seen that when the applied current surpassed a certain threshold, the resistance was reduced; the trimmed resistance was stable under the current lower than the threshold and decreased with the further enhancement of the trimming current. This phenomenon only exists in the polycrystalline silicon films with the doping concentration higher than 1×10^{20} cm^{-3}.

The experimental results presented by Amemiya et al. indicated that the carrier concentration was invariable and the mobility