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Possible new mechanism of chip latent damage due to ESD

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ABSTRACT

This paper introduces a possible new, to-date not recognized mechanism of microelectronic chip damage due to ESD as well as numerical simulation of some corresponding damage scenarios for an ESD protection device.
The model presented herein recognizes the effects of thermo-mechanical coupling that can produce excessive mechanical stresses, elastic shock waves and mechanical damage in a chip during an ESD event. This mechanism can get activated at temperatures well below melting point and thus may be an early contributor to latent and "hard" ESD failures.

1. Introduction

ESD is one of the major reliability problems associated with integrated circuits (IC). In order to prevent chip damage by the large amplitude currents, practically all ICs have built-in protection circuits, which shunt to the ground the electric charge caused by ESD. The present design methods of ESD protection recognize electrical breakdown and thermal melting as the primary mechanisms damaging the chip [1–3]. However, in many cases some damage occurs before the temperatures in the device have reached the melting point [1,4,5], which indicates that there may be another factor contributing to chip failure in presence of transient high temperatures associated with ESD pulses.

In this paper we present a new mechanism that is a likely contributor to chip damage due to ESD, especially to the so-called latent damage (we are referring to "latent" or "soft" as damage that may cripple the performance of the ESD protection device without outright and visible destruction, or that may require several cycles of application to produce perceptible flaws in the device). This mechanism takes into account the high thermo-mechanical stress levels caused by local thermal expansion, combined with a possibility of elastic shock waves and dynamic vibrations triggered by the transient nature of ESD spikes. The resulting mechanical stresses can reach high enough values to exceed the strength of the chip materials and cause damage of the silicon, the oxide layer or delamination of different films that are part of an IC.

2. Thermo-mechanical mechanism of chip damage

According to the proposed thermo-mechanical mechanism, the sequence of events at an ESD instance is as follows:

1. ESD causes a large current to pass through a protective circuit. This in turn causes local heating, which occurs very fast and within very small volumes.
2. The local heating causes, through thermal expansion of materials, intense mechanical stress.
3. Depending upon the rate of temperature increase, mechanical vibrations or elastic waves may be triggered in the device, further compounding mechanical stress intensity. This will be most likely for faster ESD events.
4. The stress intensity caused by thermo-mechanical effects may surpass the strength of the chip materials and/or interfaces between different layers, leading to plastic dislocations, cracking and/or delamination.

Furthermore, the mechanical cracks and delamination may provide an additional barrier to current flow and/or heat dissipation in consecutive ESD events and thus precipitate further destructive effects.

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The analytical description of the above thermo-mechanical mechanism follows standard equations of solid mechanics with thermal loading – a brief version is presented in [6].

3. Numerical simulation

In order to investigate the feasibility of ESD protection failure via the mechanism put forth in this paper, a specialized simulation software package has been developed. The overall sequence of such simulations is as follows:

1. Perform electro-thermal simulation of an ESD event using commercial IC simulation software (in this work TCAD™ package from Integrated Systems Engineering was used). The main parameter of interest produced by this software is the history of temperature field in the chip.
2. Using the temperature history as input, perform thermo-mechanical stress simulation. This includes examining the mechanical stress level within the chip in order to assess the potential of damage, such as cracks, delamination of material interfaces, or dislocations.

The respective thermo-mechanical simulation capability was implemented within a three-dimensional adaptive finite element software package PHLEX [7] from Altair Engineering.

4. Examples

The potential of thermo-mechanical damage was studied using an example of a rather classical GGMOS protection circuit subjected to an ESD event. The cross-section of this device with identification of respective materials is shown in Fig. 1. The corner regions at material interfaces have been rounded in order to better represent the typical effect of deposition/etching sequences – this also avoids artificial stress concentrations typically produced by sharp corners.

The width of the device is 1.75 μ and the width of the Gate Polysilicon is 1.0 μ. The total area included in the simulation (covered by the finite element mesh) is 4.4×4.4 μ. The length (in the plane normal to the mesh) is assumed to be very large compared to device width, so that the electrical current and heat distribution are uniform along the length. Hence, a 1 μ segment of representative length is considered in the simulation.

The device was subjected to an ESD event. The electro-thermal aspects were simulated using the commercial package Dessis™ from ISE TCAD. In the context of this work the most important aspects of this simulation are the history of temperature and the spacial distribution of temperature, as illustrated in Fig. 2. Importantly, the *temperature distribution is still well below melting.*

The history of temperature was then transferred to PHLEX for thermo-mechanical analysis. The two-dimensional mesh from

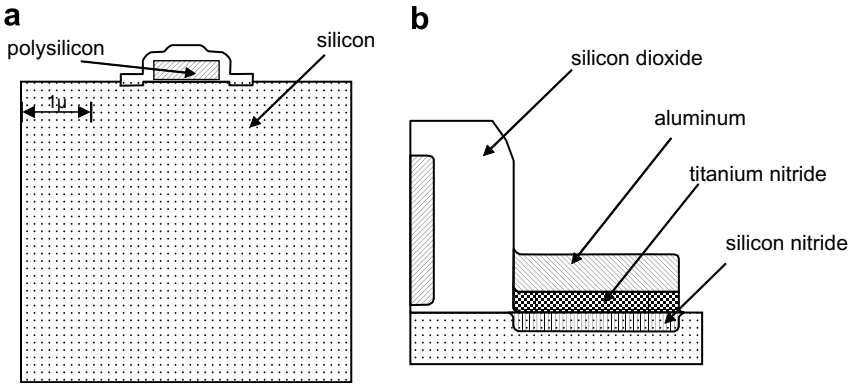

Fig. 1. Device cross-section and material components.

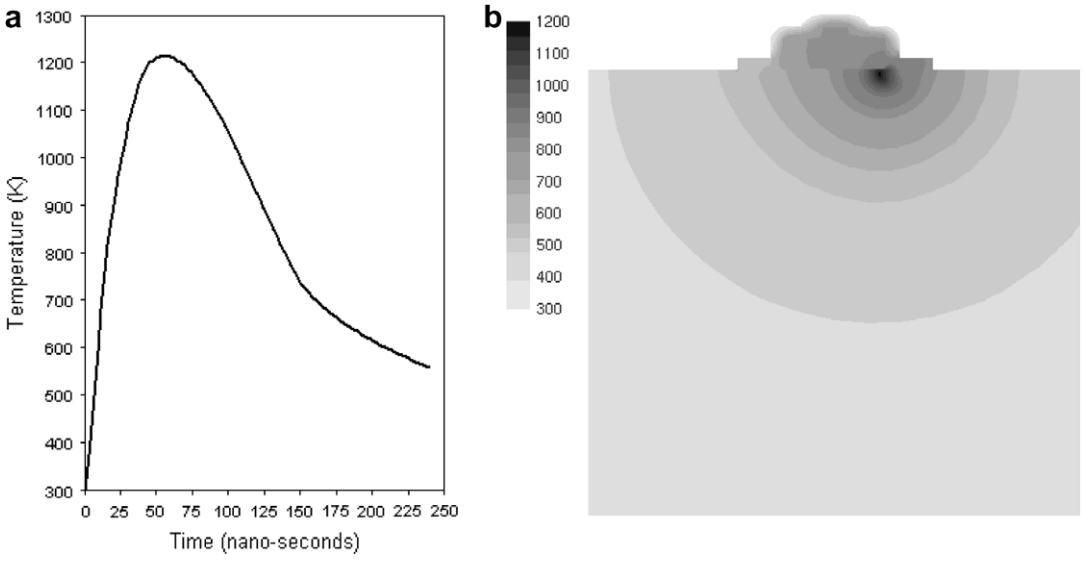

Fig. 2. History of maximum temperature during an ESD event and the distribution of temperature during peak heating.