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Influence of inhomogeneous contact in electrical properties of 4H–SiC based Schottky diode

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ABSTRACT

Schottky diodes realized on 4H–SiC n-type wafers with an epitaxial layer and a metal-oxide overlap for electric field termination were studied. The oxide was grown by plasma enhanced chemical vapor deposition (PECVD) and the Schottky barriers were formed by thermal evaporation of titanium or nickel. Diodes, with voltage breakdown as high as 700 V and ideality factor as low as 1.05, were obtained and characterized after packaging in standard commercial package (TO220).

The electrical properties such as ideality factor, hight barrier, the series resistance R_s were deduced by current/voltage (I–V) analysis using the least mean square (LMS) method. The temperature effect on break voltage, R_s and saturation current was studied. A model based on two parallel Schottky diodes with two barrier heights is presented for some devices having an inhomogeneous contact. It is shown that the excess current at low voltage can be explained by a lowering of the Schottky barrier in localized regions. We use the two series RC components electrical model in order to study the dynamic behaviour of the Schottky diode in low frequency and to improve the effect of barrier inhomogeneities in electrical properties.

1. Introduction

Silicon carbide is considered as the semiconductor material that will enable the transition of traditional silicon power electronics into smart power. Silicon carbide has material properties that allow devices with higher voltage rating and higher operating temperatures compared to traditional silicon, which translates into smaller and less expensive components.

The physical properties make SiC a semiconductor of choice for electronic applications in which high temperature, high voltage, high frequency and/or high power are involved. Devices made by silicon carbide were realized for power Schottky diodes and MOSFET's [1,2].

One of the most important problems in industrial application of SiC is the low quality of the material compared to classical semiconductors such as silicon. The presence of defects, such as micropipes, dislocations, comets and inclusions of different polytypes in the epitaxial layers, can give effects on devices performances or failures [3]. Various phenomena have been considered to be responsible for Schottky barrier height inhomogeneities. For example, difference in the crystal symmetry of the metal with respect to the semiconductor or variation in the orientation at the metal-semiconductor interface, due to localized faceting of the interface has been observed [4]. Doping inhomogeneity, dopant clustering, contaminations are other features which can lead to Schottky barrier inhomogeneities [5].

The present paper reports on Schottky diodes realized on 4H–SiC n-type wafers with an epitaxial layer and a metal-oxide overlap for electric field termination. The oxide was grown by plasma enhanced chemical vapour deposition (PECVD) and the Schottky barriers were formed by thermal evaporation of titanium or nickel. The main electrical properties (such as ideality factor, height barrier and series resistance) were extracted by current/voltage (I–V) analysis using a least mean square method and considering different approximations. The dynamic properties were studied by capacitance measurements and correlated to the properties of Schottky diode.

2. Experimental details

Schottky diodes were realized from SiC wafers with a 7-µm thick lightly doped (10^{15} cm^{-3}) n-type epilayer grown on highly doped (10^{19} cm^{-3}) Si-face 4H–SiC substrate, commercially available from Cree. A thin film of silicon oxide was grown on epilayer by standard 13.56 MHz plasma enhanced chemical vapor deposition (PECVD) by a mixture of CO_2, SiH_4 and H_2. The growth conditions and the post deposition treatment have been chosen so as to

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optimize SiO_2 properties [6]. After silicon dioxide growth, a guard ring was realized by standard lithography processes. Schottky barrier formation on 4H–SiC epilayer was obtained by thermal evaporation. We have used titanium or nickel, with or without thermal annealing in controlled atmosphere (under N_2 flow). For titanium the annealing temperature was 400 °C, for nickel 350 °C. A metal-oxide overlap for electric field termination was realized. Ohmic contact formation was made on the back of the wafer by a sequential evaporation of titanium, nickel and silver for all the samples.

The electrical properties were extracted from *I*–*V* analysis, performed in the cryogenic system by an electrometer Keithly 6517A, in temperature range varying from 10 K to 460 K. The dynamic properties were studied by the capacitance variation versus frequency and voltage bias measured by using HP 4274A (100 Hz–100 kHZ) LCR meter and HP 4192 (1 kHz–1 MHz) impedance analyser.

3. Results and discussion

3.1. Current and voltage characterizations

Schottky diodes in the structure given by Fig. 1 were realized on analyzed wafers electrically and structurally characterized [7]. Forward *I*–*V* analysis has lead to the determination of the characteristic parameters of the devices, such as the Schottky barrier height (ϕ_B), the ideality factor (n) and the series resistance (R_s).

Fig. 2 reports electrical characteristics of Schottky diode with barrier in titanium annealed at 400 °C at different temperature varying from 10 K to 460 K. In low temperature, the density of current decreases and the turn on voltage increases. Two different trends are observed. Under temperature of 300 K, a small deformation appears showing that a two Schottky barrier height behavior may be observed at lower temperature. This phenomena was observed by Defives et al. [3]. With increasing temperature, the current density increases, the turn on voltage decreases and the characteristic tends to the one Schottky barrier height trend. Therefore the excess current appears at low temperatures and disappears at higher temperatures. The barrier height increased with increasing the temperature (Table 1). It passes from 0.76 eV at 10 K to 1.26 eV at 460 K. This may be due to the shift in Fermi level with activation of shallow carriers due to variation of the temperature.

The ideality factor n incorporates all those unknown parameters making the device non ideal [8]. A Schottky diode is unlikely to be uniform over its entire area. The value of n is higher than 1 as given in Table 1 and decreases with increasing temperature. A small variation of ideality factor n gives the evidence that current is not dominated by recombination current [9].

Reverse *I*–*V* measurements were utilized to obtain the breakdown voltage (the value of reverse voltage at 1 mA of reverse current). The improvement of barrier height with annealing gives also a significant improvement in values of voltage breakdown as it can be seen in Table 2. From Fig. 3, we can deduce that breakdown voltage decreases with increasing temperature. It passes from 875 V at 70 K to 489 V at 460 K. Two slopes of breakdown voltage were found. Devices with barrier in titanium show breakdown voltage up to 600 V and the non reversible breakdown voltage 850 V was found. The slope variation of breakdown voltage changes from small temperature range between 70–250 K and high range 270–460 K.

3.2. Methods and models

We utilize the least mean square method (LMS) to extract the parameters of Schottky diodes by using the predetermined analytic function describing the experimental data [10].

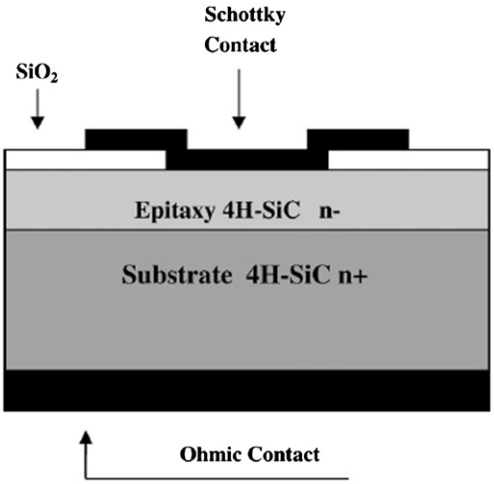

Fig. 1. Structure of studied Schottky diode.

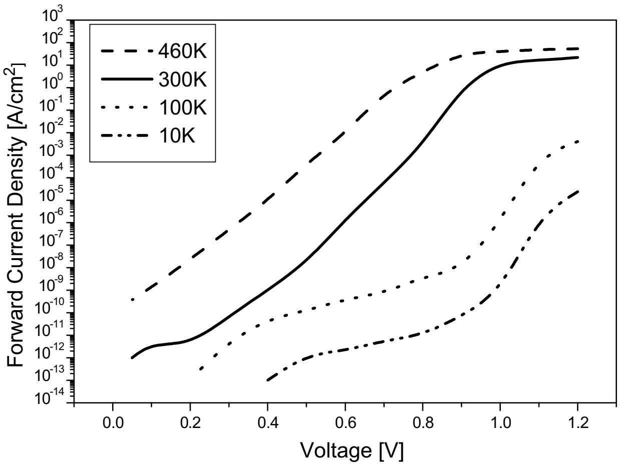

Fig. 2. Forward current density *J* versus Voltage at different temperature for diode in Ti ann. 400 (TO220).

Table 1
Ideality factor and barrier heights versus temperature of studied Ti ann. 400 Schottky diode using Method 1

Temperature [K]	n	ϕ_B [eV]	Qlms [%]
10	1.26	0.76	0.26
50	1.22	0.81	0.20
100	1.21	0.92	0.17
150	1.18	0.95	0.16
200	1.17	0.99	0.18
250	1.15	1.01	0.13
300	1.14	1.00	0.09
350	1.13	1.13	0.07
400	1.10	1.21	0.08
460	1.07	1.26	0.09

In practice we consider the model, used in the p–n junction diode, and give the current I versus voltage polarisation V:

$$I = I_s\left[\exp\left(q\frac{V - R_s I}{nkT}\right) - 1\right] \tag{1}$$

where I_s the reverse saturation current, n the ideality factor, R_s the series resistance.