Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 52 (2008) 99–106
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Explicit compact model for symmetric double-gate MOSFETs including solutions for small-geometry effects

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Received 23 January 2007; received in revised form 14 May 2007; accepted 21 June 2007
Available online 9 August 2007

The review of this paper was arranged by Prof. A. Zaslavsky

Abstract

A physics-based compact model including short-channel effects (SCEs) is presented for undoped (or lightly doped) symmetric double-gate (DG) MOSFETs. Our approach allows an accurate description of the device behavior down to 60 nm with a simple set of equations. It is shown that the subthreshold current, the threshold voltage roll-off and the DIBL predicted by the analytical solution are in close agreement with 2-D numerical simulations performed with Atlas. The mobility degradation due to both transverse and longitudinal fields is taken into account but the channel length modulation (saturation regime) is not addressed in this paper. In order to demonstrate that the model is well-suited for circuit simulation, the results of the dynamic model based on an explicit formulation of the mobile charge density are also presented.

Keywords: DG MOSFET; Compact model; Short-channel effects (SCEs); DIBL; Threshold voltage; Roll-off

1. Introduction

The double-gate MOSFET is considered to be one of the most promising device structures to extend CMOS scaling into the nanometer regime [1]. DG MOSFETs can be scaled to the shortest channel length possible for a given gate oxide thickness [2]. The advantages of DG MOSFETs include: ideal 60 mV/dec subthreshold slope [3], scaling by silicon film thickness without high doping, setting of threshold voltage by gate work functions [4], etc. The key factors that limit how far a DG MOSFET can be scaled come from short-channel effects (SCEs) such as threshold voltage roll-off and drain-induced barrier lowering (DIBL). As far as short-channel effects are concerned, several models have been published [5–9]. Among them, the solution brought by [9], based on the general scale length analysis made in [10] presents strong physical basis, since no assumption is initially made on the potential profile into the channel. However, the drain current is given in an integral form, which can only be solved by numerical calculation.

In this paper, we present an accurate and explicit compact model for the symmetric double-gate MOSFET. All the approximations introduced in this work are discussed in order to provide a physics-based compact model. We put forward an accurate formulation of the short-channel effects in subthreshold region that allows us to predict the behavior of deca-nanometer devices. The presented approach takes into account the carrier velocity saturation within the mobility model, but the channel length modulation is not

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doi:10.1016/j.sse.2007.06.020

included yet. The modeling of saturation regime, quantum effects and extrinsic capacitances are beyond the scope of this paper. The paper is organized as follows. In Section 2, we briefly describe the core of the explicit long-channel model that has already been developed in our previous works [11,12]. Section 3 details the modeling of small-geometry effects such as: subthreshold swing, threshold voltage roll-off, DIBL and mobility degradation. Finally, in Section 4, the results of the compact model are compared with 2-D numerical simulations.

2. Long-channel model

In our previous works [11,12], we proposed a design oriented charge-based model for undoped DG MOSFETs under symmetrical operation that aims at giving a comprehensive understanding of the device from the design strategy. By emphasizing the link between this approach and the EKV formalism derived for bulk MOSFET, we introduced useful normalizations for current and charges that in turn lead to very simple relationships among the physical quantities [11]. Then, we proposed a robust algorithm for computing the mobile charge density as an explicit function of the terminal voltages. It has allowed to greatly reduce the computation time without losing any accuracy [12]. The model continuously covers all operation regions and is in excellent agreement with 2-D numerical simulations without any fitting parameters.

The main assumptions of the long-channel model are the following: the silicon layer is lightly doped, the mobility is constant along the channel and both polydepletion and quantum effects are neglected. The last assumption is valid for silicon layer thicknesses down to at least 10 nm. Quantum confinement effects start to become significant in devices with silicon film thickness smaller than 5 nm. The incorporation of quantization to the classical solution for the distribution of the electric potential, which results in an increase of the channel surface potential from the classical result [13,14], will be subject for a future work. The schematic diagram of the DG MOSFET considered in this work is shown in Fig. 1.

For the sake of clarity, we now briefly describe the major results that led to the derivation of the drain current

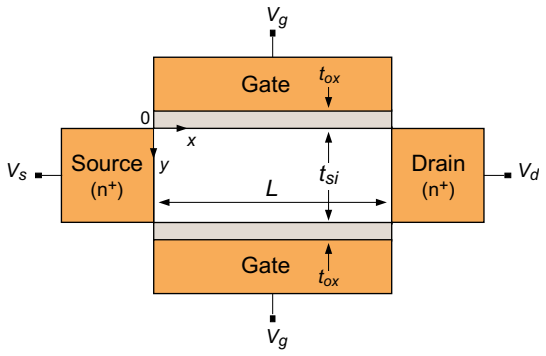

Fig. 1. Schematic of the DG MOSFET structure investigated in this work.

model. Using the normalization of charges, potentials and current proposed in [11], leads to an important relationship between charge densities and potentials, given by:

$$v_g^* - v_{ch} - v_{to} = 4 \cdot q_g + \ln q_g + \ln\left(1 + q_g \cdot \frac{C_{ox1}}{C_{Si}}\right). \tag{1}$$

Introducing the concept of pinch-off voltage, (1) can be rewritten as:

$$v_p - v_{ch} = 4 \cdot q_g + \ln q_g + \ln\left(1 + q_g \cdot \frac{C_{ox1}}{C_{Si}}\right), \tag{2}$$

where $v_p = v_g^* - v_{to}$ is the pinch-off voltage, v_g^* is the effective gate voltage ($=v_g - \Delta\phi_{mi}$ with $\Delta\phi_{mi} = \Delta\phi_{MI}/U_T$ the normalized work function difference between the gate electrode and intrinsic silicon), v_{ch} is the electron quasi-Fermi potential, q_g is the charge density per unit surface of each gate, C_{ox1} is the gate oxide capacitance per unit surface of each gate, C_{Si} is the silicon layer capacitance per unit surface and v_{to} is the threshold voltage. The v_{to} value corresponds to the long-channel threshold voltage. It is defined as the gate voltage where the mobile charge density vanishes as extrapolated from strong inversion [11]. Therefore, we obtain:

$$v_{to} = \Delta\phi_{mi} - \ln\left(\frac{e \cdot n_i \cdot t_{Si}}{4 \cdot C_{ox1} \cdot U_T}\right), \tag{3}$$

where e is the electronic charge, n_i the intrinsic carrier concentration and $U_T = k \cdot T/e$ the thermal voltage.

Such a normalization represents an efficient tool for the analog designer because it is done taking into account the design methodologies requirements [15]. However, (1) needs to be solved numerically and this is not desirable for circuit simulation (it requires at least several iterations). To overcome this drawback, we have developed a new methodology to compute without any iteration the mobile charge density as an explicit function of bias voltages (v_g and v_d or v_s) [12,16]

$$q_g = f(v_g, v_{ch}) \quad \text{with } v_{ch} = v_s \quad \text{or} \quad v_d. \tag{4}$$

Without entering into details, the numerical inversion of (1) can be performed using a reduced set of precomputed parameters that depend only on the so-called "form factor" $\alpha = C_{ox1}/C_{Si}$. Let us emphasize that our algorithm of numerical inversion fully preserves the physics of (1), and therefore its validity is technology-independent [12,16]. Then, noting that the mobile charge density is twice the gate charge density ($q_m = -2 \cdot q_g$) and assuming that the drift-diffusion transport model is valid, the normalized drain current i can be expressed as:

$$i = -\int_{v_s}^{v_d} q_m \cdot dv_{ch}. \tag{5}$$

Integrating (5) from source to drain yields:

$$i = -q_m^2 + 2 \cdot q_m + \frac{2}{\alpha} \cdot \ln\left(1 - \alpha \cdot \frac{q_m}{2}\right)\Bigg|_{q_{mS}}^{q_{mD}}. \tag{6a}$$