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High-temperature enhancement mode operation of n-channel GaN MOSFETs on sapphire substrates

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Abstract

The high-temperature operation of a GaN MOSFET is reported. The MOSFETs were operated up to 250 °C, best reported to date. The MOSFETs showed good dc characteristics with field-effect mobilities of 138 cm^2/Vs and 133 cm^2/Vs at room temperature and 250 °C, respectively. The field-effect mobility, threshold voltage, and sub-threshold slope did not changed significantly up to 250 °C. Also, we compared the activation annealing condition for n^+ layer fabrication. A high-temperature annealing condition of 1300 °C led to a low contact resistance, but caused slight degradation of the field-effect mobility compared with the 1100 °C annealing condition.

Keywords: Enhancement-mode; Gallium nitride; High-temperature operation; MOSFETs

1. Introduction

Silicon transistors for power electronics, such that power metal-oxide-semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), have been constantly progressing. Recently, however, their performance is moving toward a limitation due to the physical properties of Si. Wide band gap semiconductors, such like gallium nitride and silicon carbide, are expected to be candidates to overcome the limitation from the physical properties of Si, because they have a high critical breakdown voltage, superior carrier transport properties, and good thermal dissipation.

Among various III–V nitride transistors, AlGaN/GaN hetero structure field-effect transistors (HFETs) have been intensively studied due to their high mobility and high-density 2-dimensional electron gas (2DEG) arising due to the piezzo effect and self-polarization charges. The high-temperature operation of an AlGaN/GaN HFET with a low on-state resistance was previously reported [1–5]. Moreover, AlGaN/GaN HFETs have a high switching speed. These characteristics of GaN transistors are very attractive for power-switching applications [6,7]. A high-temperature, low loss switching operation of the HFET enables one to reduce the complexity of the cooling systems in power electronics applications.

Studies of the AlGaN/GaN HEMT started from a normally on operation. However, a normally off operation is required from system sides because of fail-safe and noise margin, which is now drawing much research attention. Many techniques, such as thin AlGaN/AlN structure [8], recessed gate structure [9,10], CF_4 based plasma treatment [11], and p-AlGaN gate structure [12], have been applied to achieve a normally off operation. However, their threshold voltage were up to 1–2 V, which is not sufficient to maintain good noise margin in the several hundred volt range.

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Another candidate of a normally off device is the GaN MOSFET. Since native oxide is not obtained on a GaN surface, various gate dielectric materials are used, such as MgO [13,14] and SiO_2 [15–18]. Among these gate dielectrics, SiO_2 has a large conduction-band offset and a large band gap, which prevent tunneling of electrons through the dielectric. A normally off GaN MOSFET with a high field-effect mobility was reported recently [19], but high-temperature operation over 200 °C and large-current operation have not yet been reported.

In this paper, we report on the fabrication of a GaN MOSFET using a high-temperature RTA technique to achieve good activation of implanted Si. We report on the high-temperature operation of GaN MOSFET up to 300 °C and large-current operation at more than 1 A for the first time.

2. Device fabrication

Fig. 1 shows a schematic cross-sectional view of the fabricated GaN MOSFET.

A p-type epi-layer and a buffer layer were grown by metal-organic chemical vapor deposition on a sapphire (0001) substrate. The thickness of the p epi-layer and highly resistive buffer layer were 2 μm and 1 μm, respectively. A p epi-layer was doped with Mg acceptor doping concentration of 1×10^{17} cm^{-3}.

After alignment mark fabrication by dry etching using BCl_3, source and drain regions were selectively ion implanted with a silicon dose of 3×10^{15} cm^{-2} and a maximum energy of 190 keV through a 20 nm SiO_2 layer deposited by plasma-enhanced chemical vapor deposition (PE-CVD) as a mask. We applied two conditions for the activation annealing of an implanted Si. Activation annealing was performed by a rapid thermal annealing (RTA) and a furnace. The sheet resistance of a sample annealed by a RTA was decreased upon increasing the temperature and time. Since the maximum setup of the temperature and the annealing time of our RTA were 1300 °C and 30 s, respectively, we chose the condition of 1300 °C and 30 s for RTA (sample A). The sheet resistance of the sample annealed by a furnace was also decreased while increasing the temperature and time, but a degradation of the surface morphology and warpage of the wafer were observed after 10 min of annealing at 1100 °C. We thus chose the condition of 1100 °C and 5 min for a furnace annealing (sample B). A 500 nm SiO_2 layer deposited by PE-CVD was used as an annealing mask. The activation ratio was almost 100% and the sheet resistance of a n^+ GaN layer was 60 Ω/square in sample A. The sheet resistance of an n^+ GaN layer was 2500 Ω/square in sample B. High-temperature rapid thermal annealing was very effective to reduce the sheet resistance of the n^+ GaN layer.

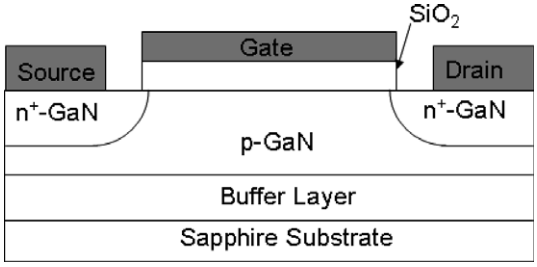

Fig. 1. Schematic cross-sectional view of a n-channel GaN MOSFET.

Table 1
Results of contact resistance and sheet resistance of sample A and sample B

	Activation annealing	Contact resistance [Ω cm^2]	Sheet resistance [Ω/square]
Sample A	1300 °C, 30 s, RTA	2.7×10^{-6}	60
Sample B	1100 °C, 5 min, furnace	2.1×10^{-5}	2500

After removing the activation mask, the wafer was cleaned by the RCA method and $HCl:H_2O$ of 1:3 for 5 min. A 60 nm thick SiO_2 layer was deposited by PE-CVD as a gate oxide and annealed at 900 °C for 30 min in N_2 ambient. This annealing technique is useful to reduce the interface state density and the densification of SiO_2 [19,20].

The source and drain regions were defined by conventional photo lithography. After opening a SiO_2 window by a BHF solution, Ti/Al was deposited by sputter equipment, and then lifted off. The source and drain contact were annealed at 600 °C for 10 min in a N_2 ambient. The contact resistance was measured by the TLM method. The contact resistance of the source and the drain electrode of sample A and B were 2.7×10^{-6} Ω cm^2 and 2.1×10^{-5} Ω cm^2, respectively. The results of n^+ layer fabrication are summarized in Table 1. The contact resistance of sample A was very low due to good activation of the implanted silicon. The gate electrode was also defined by photo lithography. Ti/Au was used for the gate electrode by the lift-off technique.

3. *I–V* Characteristics at room temperature

Fig. 2 shows typical output *I–V* characteristics of the circular GaN MOSFET sample A with a channel length of 4 μm and a channel width of 1 mm at room temperature. Note that the maximum current of the measurement setup was controlled to 0.1 A. Good output characteristics were observed. Figs. 3 and 4 show a linear plot and a log plot of typical transfer *I–V* characteristics of the GaN MOSFET at room temperature, respectively. The threshold voltage of the GaN MOSFET was 0.7 V. A maximum field-effect mobility of 138 cm^2/Vs was observed, which is close to the value previously reported [18,19]. The maximum current was more than 100 mA/mm. This high-current density arises from a low contact resistance, low sheet resistance, and good field-effect mobility. Good linearity of the V_{gs}–I_{ds} characteristics show that the effect of the interface state of the density was sufficiently small. A sub-threshold slope