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Bias-stress induced threshold voltage and drain current instability in 4H–SiC DMOSFETs

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Abstract

In this work, the instability of n-channel 4H–SiC double-implanted metal–oxide–semiconductor field-effect-transistors (DMOSFETs) was studied, in terms of threshold-voltage (V_{TH}) shifts and drain–source current (I_{DS}) transients, for different gate bias stress durations of range 100–5500 s. At room temperature, for positive gate bias stress, the V_{TH} shift and I_{DS} decay increase with increasing stress time. The V_{TH} shift and the I_{DS} decay were recovered by negative gate bias stress. It is believed that the instability in device behavior during positive gate bias stress is due to capture of electrons by the SiC/gate dielectric interface traps and the gate dielectric near interface traps. Elevated temperature measurements have indicated a decrease in V_{TH} and an increase in I_{DS} with increasing stress time possibly due to mobile positive ions in the gate dielectric.

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Keywords: SiC; DMOSFET; Threshold-voltage shift; Drain current transient; Interface traps; Mobile ions

1. Introduction

Silicon carbide (SiC) has several potential material advantages over Si for the development of high-power solid-state devices. These advantages include a wide band-gap, a large critical field, and a large thermal conductivity, which all together make SiC as an attractive material for high power and high frequency applications [1–3]. Though, SiC DMOSFETs are beginning to be commercialized [4], there are still a number of issues that need to be solved to improve the performance of SiC DMOSFETs. The issues, attributed to the high density of SiC/SiO_2 interface traps and near-interface traps [5,6], are a negative threshold voltage (normally-on) [7–9], a low inversion-channel carrier mobility [10], reliability issues [11–13], and threshold-voltage instability [14,15].

In this work, the threshold voltages of SiC DMOSFETs were measured after different bias stress durations to determine if the bias stress induces a shift in the threshold voltage. The bias stress measurements were also performed at elevated temperatures. The problem with using threshold-voltage drift measurements alone as an indicator of magnitude of device instability is the lack of consensus on the definition of threshold voltage for SiC DMOSFETs (as described in the next paragraph). In addition, if measurement sweep time to acquire transfer curves at the conclusion of bias stress is long, the electrons may be trapped or detrapped during the sweep also, which may result in altered transfer curves and consequently an erroneous extraction of V_{TH}. Recent measurements by Gurfinkel et al. [16], driven by the interest in faster measurement,

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have shown a clear dependence between the measured magnitude of instability and the speed of the measurement. Due to this reason, in this work, in addition to studying the threshold-voltage drift, we have also concentrated on studying the drain current transients during the stressing period at both room temperature and elevated temperatures to see if monitoring of the drain current transient during stressing can be used to study the SiC DMOSFET instability. A detailed description of DMOSFET's device operation is given in Ref. [17].

Since SiC DMOSFET's turn-on drain current (I_{DS}) increase with increasing gate–source voltage (V_{GS}) is rather gradual, unlike in Si MOSFET's, there is not a widely accepted threshold-voltage (V_{TH}) definition available for SiC DMOSFETs. Thus, in this work, based on the i_{DS}–v_{GS} transfer characteristics obtained at $V_{DS} = 0.1$ V, the V_{TH} is defined in three ways: (1) V_{TH_SQRT}, which is the v_{GS}-axis intercept of a linear fit to the 90% and the 60% values of $\sqrt{I_{DS}}$ at $V_{GS} = 15$ V, (2) V_{TH_LIN}, which is the v_{GS}-axis intercept of a linear fit to the 90% and the 60% values of I_{DS} at $V_{GS} = 15$ V, and (3) V_{TH_LOG}, which is defined as the V_{GS} value at a drain current of 1×10^{-8} A.

2. Experiment

The SiC DMOSFETs were fabricated on a 11 μm thick n-type epitaxial layer (3.5×10^{15} cm^{-3}) grown on an n-type 4H–SiC substrate. A schematic of the DMOSFET cell structure is shown in Fig. 1. Each DMOSFET of this work has 625 such cells. The p-well is formed with a multiple energy aluminum implant. Source region was implanted with nitrogen, and a body contact region was co-implanted with aluminum and carbon. The wafer was capped with graphite and annealed for 30 min at 1675 °C for activating the implants. The graphite was removed with an ashing process and the SiC surface was further prepared by thermally growing a 300 Å thick sacrificial oxide. The sacrificial oxide is thermally grown to remove (consume) a thin (~130 Å) layer of SiC wafer surface, which may have defects created in it during graphite cap deposition, implant annealing, and cap removal steps. A 50 nm thick gate oxide was grown by successive 1250 °C (in N_2O) and 1175 °C (in NO) oxidation steps immediately after etching the sacrificial oxide. A liftoff process was used to form nickel ohmic contacts to both n^+-type and p^+-type regions. A 0.6 μm thick molybdenum gate metal was deposited and patterned and then the ohmic contacts were annealed at 1050 °C for 3 min. The devices were passivated with a silicon nitride film.

Bias stress measurements on the SiC DMOS devices were performed using a Hewlett Packard (Agilent) 4142B Modular DC Source/Monitor Unit and the Metrics Interactive Characterization Software (ICS), version 3.6.0.

A typical cycle used for the bias-stress induced threshold voltage and drain current instability measurements, shown in Fig. 2a, consists of four different gate biasing steps in the order: (1) keeping the gate–source voltage (V_{GS}) at +15 V (positive-stress) for a certain duration, (2) V_{GS} sweep from +15 V to −15 V (sweep-down), (3) keeping V_{GS} at −15 V (negative-stress) for the same amount of duration as the positive-stress, and (4) V_{GS} sweep from −15 V to +15 V (sweep-up). During the entire cycle the drain–source voltage (V_{DS}) was kept small at 0.1 V, which ensures operation of the device in linear region. The Hewlett Packard 4142B with fast integration setting takes about 2 s to perform sweep-down and sweep-up (from +15 V to −15 V and −15 V to +15 V, respectively, with increments of 0.1 V). The sweep time of 2 s is relatively slow compared to ones reported for the threshold instability measurements (10 μs–1 s) [14–16]. At the end of each step in the bias-stress cycle, all terminals were returned to 0 V and it took about 2 s to setup and start the subsequent step.

First, the bias-stress induced threshold-voltage instability measurement was performed for a 180 s of stress dura-

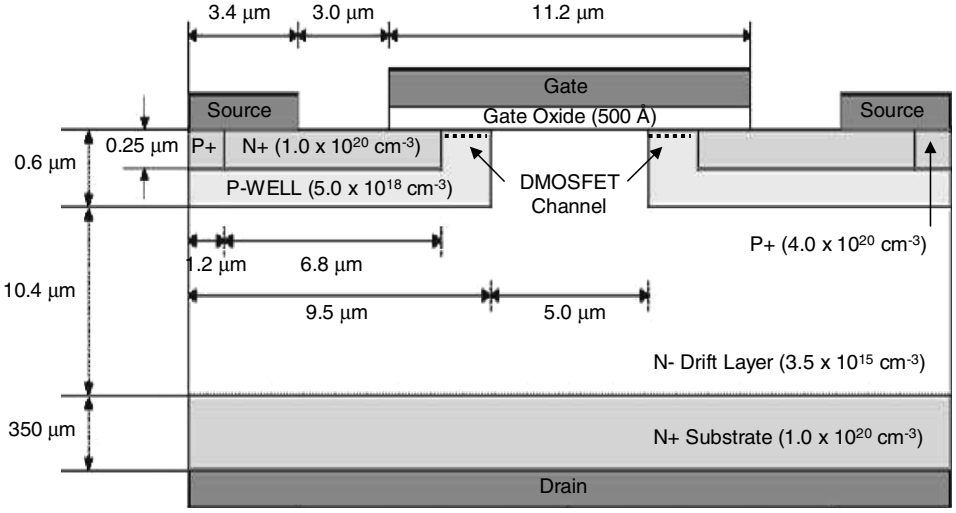

Fig. 1. Schematic of the DMOSFET cell structure.