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Research directions in beyond CMOS computing

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Abstract

The International Technology Roadmap for Semiconductors has identified five promising research directions in beyond CMOS computing technology that are discussed here. Alternate state variables beyond electronic charge are introduced. Momentum and spin relaxation times for electrons in GaAs are calculated and show that magnetic systems are less strongly coupled to the thermal environment than systems based on electronic charge.

Keywords: Nanoelectronics; Transistor; Power dissipation; Non-equilibrium; Spintronics; Self-assembly

1. Introduction

The capability of computing technologies has increased an astonishing 12 orders of magnitude during the 20th century and gone through several distinct paradigm shifts beginning with electromechanical relays, vacuum tubes and semiconductor based processors. At the beginning of the 21st century, we are at the threshold of another paradigm shift opened up by the ability to mass manufacture structures with nanometer dimensions and picosecond operational times. The semiconductor industry is spending tens of billions of dollars on developing ultimate CMOS devices and is partnering with national governments around the world in the search for computing technologies beyond CMOS and electric charge based devices. These longer range research activities amount to approximately 1 billion dollars a year worldwide and are concentrated in the US, Europe and Japan.

Intel Corporation is playing a leadership role in the development of ultimate CMOS devices and in the search for beyond CMOS devices that will extend continued improvement in cost per function as described by Moore's law even further. We believe that scaling of more or less conventional MOSFET devices will continue for at least 15 years and that any future technologies beyond CMOS will be tightly integrated with and created on CMOS platforms.

As CMOS and other charge based devices approach scale lengths of 10 nm and operational times of a picosecond, quantum mechanical effects will assume greater importance. The influence of tunneling and quantization have long been recognized but will become relatively more important. At the extreme scale lengths we will be encountering over the next 20 years additional new physical effects will come into play.

One significant paradigm shift we are facing is that future devices will be smaller and faster than the scale lengths necessary to establish local thermodynamic equilibrium. In silicon, these scales are of the order of 10 nm and picosecond equilibration times. This will have dramatic effects in nanoscale thermal management and some indications of non continuum heat transport are already appearing in 90 nm transistors. However, being out of thermal equilibrium also has implications for the ambient noise field affecting device operation and may permit such nanoscale devices to operate with lower noise margins and lower energy dissipation than would otherwise be possible.

The paper's primary focus will be on the research activities relating to non charge based computing technologies organized around the five research vectors adopted by

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the International Roadmap for Semiconductors (ITRS) and the Nanoelectronics Research Initiative (NRI). It will explore the tight coupling that exists between the use of alternative computational state variables, non-equilibrium systems, novel coupling methods and thermal transport citing numerous examples from the current literature.

The overall conclusion is that a great deal of room exists for continued scaling of CMOS and beyond silicon transistors. Beyond that, the situation becomes speculative and there is presently no viable alternative to CMOS based computing visible in the research community. However, there is considerable consensus on the research directions to follow and a great deal of effort being devoted to that end around the world.

2. Computing technologies beyond CMOS and electronic charge

Current 65 nm transistors have a power delay product of approximately 2500 eV [1], which is approximately equivalent to 10^5 kT, where k is the Boltzmann constant and T is 300 K [2]. Experimental 10 nm gate length transistors have been fabricated and measured to show a power delay product of approximately 1.8 eV [1] or approximately $75kT$. The trend line connecting those two points intersects a large number of other published experimental results for devices of 100 nm gate length and larger. If one extrapolates this trend line to an extreme value of 1.5 nm gate length devices, it yields a power delay product of approximately $3kT$ or 78 meV as shown in Fig. 1. The dynamic switching energy dissipated in switching the devices is only one element of an integrated circuit's total power consumption. Other losses are associated with interconnects and clocking are significant and must be evaluated. However as a starting point, we will focus on switching energy as a metric for device performance.

A theoretical analysis [3] considers a highly simplified one-dimensional model of a bistable electronic switch consisting of two quantum wells separated by an energy barrier. At room temperature and thermodynamic equilibrium, the analysis yields a minimum barrier thickness of

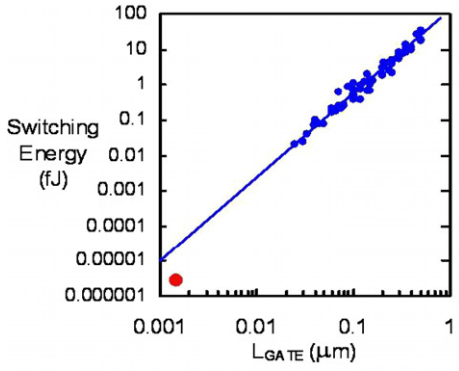

Fig. 1. Switching energy vs. gate length for a number of published NMOS transistors. A circle in the bottom of the plot indicates a derived switching energy for a highly simplified 1.5 nm bistable electronic structure described in [3].

1.5 nm for a bit error rate of 0.5. The same analysis yields a power delay product of $kT = 26$ meV, which if extended to three dimensions, yields a power delay product of $3kT = 78$ meV. Coincidentally, a series of papers by Landauer [4] concludes that the minimum energy of computation for devices at thermal equilibrium with the environment is also kT log 2 based on arguments involving entropy and irreversibility. Taken together, these papers suggest a conclusion that the minimum energy of any electronic switching device at thermal equilibrium with a room temperature heat reservoir will have a minimum gate length of 1.5 nm and dissipate approximately kT of energy per switching operation. These papers also suggest that generic CMOS devices such as those represented by the data points in Fig. 1 operate close to optimum efficiency for any bistable electronic switch operated at thermal equilibrium with a 300 K thermal reservoir. The clear inference is that the search for alternative logic devices potentially more energy efficient than the scaled CMOS must focus on devices that can operate out of equilibrium with the thermal environment.

Because electrons are so strongly coupled to the thermal background via Coulomb interaction, alternative computational state variables other than electronic charge (e.g. spin state, molecular state, phase, etc.) must be investigated to understand their coupling to the thermal background. In order to allow devices based on alternative state variables to communicate with other logic devices and support input/output operations, the search for alternative state variables must also be coupled to the search for novel energy and information transport mechanisms.

Largely motivated by the thinking outlined above, the ITRS [5] and the NRI have published a set of five research vectors to guide the research community in the search for beyond CMOS and other electronic devices. The five research vectors are listed below and discussed in the remainder of this paper.

2.1. Computational state variables other than electronic charge

The most basic element of a binary computer is a bistable structure which can store computational state. There are many physical means of representing computational state that have been used in the past including positions of beads on a wire, marks on a piece of paper, fingers, etc. Modern microelectronics rests on the use of electronic charge or electronic current to store computational state. However, based on the arguments in the preceding paragraph, it appears that going forward we may need to consider other ways of storing computational state. These alternative ways of representing state include spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration and other quantum states.

The primary motivation for considering computational state variables other than electronic charge is to look for computational switching devices that may dissipate less