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Modeling of MOSFET parasitic capacitances, and their impact on circuit performance

Judith Mueller [a,*], Rainer Thoma [a], Ertugrul Demircan [c], Christophe Bernicot [b], Andre Juge [b]

[a] *Freescale Semiconductor, 870, rue Jean Monnet, 38926 Crolles Cedex, France*
[b] *STMicroelectronics, 870, rue Jean Monnet, 38926 Crolles Cedex, France*
[c] *Freescale Semiconductor, 3501 Ed Bluestein Boulevard, MD: K10, Austin, TX 78759, USA*

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Abstract

We study layout dependent, parasitic capacitance contributions of MOSFETs with 3D simulations, and show that these contributions are for narrow and short devices comparable to intrinsic contributions. The performance of 65-nm technology is strongly affected by these components, and should therefore be modeled accurately in circuit simulations. We propose a methodology how to accurately and consistently model them in a design flow. The methodology is validated with ring oscillator measurements.
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1. Introduction

With the scaling of transistor dimensions extrinsic, or layout dependent, parasitic capacitance contributions, such as poly-to-contact coupling, as well as corner capacitance, become more and more important with respect to intrinsic contributions [1]. For 65-nm technology leaving out these contributions, can change ring oscillator delay by more than 20%. The impact on 45-nm technology is expected to be even stronger. It is therefore of utmost importance to characterize and model these parasitic capacitance contributions correctly. Today's compact models, such as BSIM, MM11, as well as PSP, distinguish channel capacitance, overlap capacitance, and fringing capacitance [2]. While the fringing capacitance takes into account the gate to source/drain coupling in the absence of contacts, it misses out on poly-to-contact coupling, and corner capacitance. Since these components depend strongly on layout parameters it is not easy to model them in a design flow. Compact models, which characterize the electrical behavior of a transistor, do not take into account layout dependent parameters. Layout parasitic extraction tools (LPE) on the other hand extract parasitic components such as coupling capacitances and resistances of metal lines, but do not consider transistors, treating them as black box. The paper is structured as follows: We first introduce the parasitic capacitance components. We show that 3D simulations, field solver as well as TCAD, are necessary to characterize these components correctly. We study their importance with respect to the intrinsic capacitance, and to better understand what influences these components we perform a sensitivity analysis with respect to several process parameters, as well as the layout parameter poly-to-contact distance. We derive equations for the extrinsic, parasitic components as a function of poly length and transistor width, which can be used in compact models. Thereafter, we discuss their impact on the delay of ring oscillators. It follows a discussion on the implementation of the

* Corresponding author.
E-mail address: judith.mueller@freescale.com (J. Mueller).

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methodology for real designs. The methodology is validated comparing ring oscillator simulation with Silicon measurements.

2. Parasitic capacitance contributions

2.1. Parasitic capacitance components

Scaling down transistor dimensions [3] such as poly length, and transistor width reduces the intrinsic capacitance and enables higher circuit performance. At the same time extrinsic parasitic capacitances such as the capacitance between gate and contact, which depends on layout parameters such as poly-to-contact distance, number of contacts, and contact spacing, do not scale in the same way. The reason is that with further increase of the density of transistor the distance between contacts and gate decreases. This reduces the access resistance, but at the same time increases the coupling capacitance. In addition corner capacitance contributions are also gaining on importance specifically for minimum transistor dimensions. Fig. 1 shows the different capacitance contributions: (1) Cox – the intrinsic capacitance, which comprises the channel-gate capacitance, and the overlap capacitance. The channel-gate capacitance scales with the poly length (L_{poly}) and transistor width W. (2) C_{fringe} – fringe capacitance, extrinsic capacitances which scales with W, poly-to-contact distances (po2con), number of contacts (N_{con}), as well as contact spacing (S_{con}), and poly length (L_{poly}). (3) C_{pc} – poly-to-contact capacitance, which depends on the transistor dimensions W, and L_{poly}, as well as on the layout parameter po2con, N_{con}, and S_{con}. (4) C_{cor} – corner capacitance, which does not depend on L_{poly}, as well as on layout parameters, such as active width, and gate extension. (5) C_{gb} – capacitance between gate and bulk, which scales with L_{poly}. This component has a voltage dependent part, which couples to the channel, and a voltage independent part. Here, we consider the voltage dependent part still as voltage independent.

2.2. Field solver simulations

Work reported in the literature so far focused on C_{fringe} to understand the scaling on L_{poly}, gate oxide height, and gate height in the absence of contacts [4,5], and on parasitic capacitance contributions such as overlap and fringing [6]. Analytic approximations with optimization parameters have been used in [7], but ignore complex geometric and material effects in advanced CMOS transistors. However, for 65-nm technology, the poly-to-contact distance reduces to 55 nm. With a gate height of 120 nm, and a contact height of 500 nm, the poly-to-contact coupling capacitance is of same order of magnitude as C_{fringe}, and cannot be ignored. Fig. 2a shows a 3D image of a transistor with its contacts, which appear like two skyscrapers next to the gate. Fig. 2b illustrates how the distribution of field lines change in the presence of contacts. The top view of the field lines motivates why 3D simulations are necessary to account for the complicated field lines between contact and gate. To evaluate the contribution of the different parasitic capacitance components 3D simulation with a commercial field solver were performed. Since the field solver can only handle metals and dielectrics, a correction factor was introduced in respective components to account for depletion/accumulation in the poly gate and active. The correction factor was obtained from TCAD simulation as described in further detail in Section 3. For the simulation in this article, we followed typical 65-nm technology dimensions, and process information for the stack. If possible the symmetry of the transistor structure was used by simulating only the half or a quarter of the structure. We verified regularly that the number of grid points were sufficient to simulate the structure. It is important to establish a good accuracy at nm-length scales since the

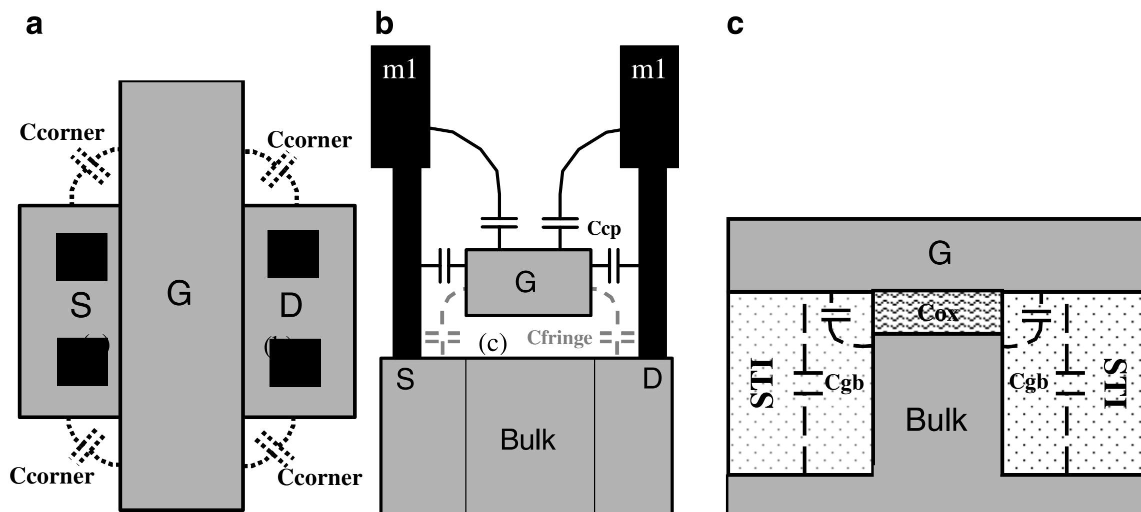

Fig. 1. Schematic of transistor with different parasitic contributions with S(ource), D(rain), G(ate), and Bulk. (a) Top view with corner capacitance (C_{cor}, dotted line), (b) cross-section along L_{poly} with fringe capacitance (C_{fringe}, dashed line) and poly-to-contact capacitance (C_{pc}, solid line), (c) cross-section along W with coupling capacitance between gate and bulk (C_{gb}, big-dashed line).

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