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Germanium FETs and capacitors with rare earth CeO_2/HfO_2 gates

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Abstract

Long channel Ge FETs and capacitors with CeO_2/HfO_2/TiN gates were fabricated by photolithography and gate wet etch. Rare earth CeO_2 in direct contact with Ge was used as a passivating layer producing lowest D_{it} values in the mid 10^{11} eV^{-1} cm^{-2} range. HfO_2 cap reduces leakage and improves equivalent oxide thickness scaling of the whole gate stack. The p-FETs show exceptionally high I_{ON}/I_{OFF} ratio $\sim 10^6$, mainly due to low OFF current, and peak channel mobility around 80 cm^2/V s. The n-FETs, although functional, show inferior performance producing ON currents an order of magnitude lower compared to p-FETs.

1. Introduction

Traditional device scaling becomes increasingly difficult due to short channel effects and increased power consumption. High mobility semiconductor channels such as Ge or III–V compounds could increase performance of devices beyond that possible with standard Si-based technologies.

Since the early demonstration of functional Ge MOSFETs with high-k gate dielectrics [1–4], substantial improvements have been made [5,6]. In particular, using buried channels made of strained-Ge, 9× enhancement in channel mobility has been achieved [6]. In addition, deep submicron Ge p-FETs on GOI have been demonstrated in a 200 mm pilot line which is good progress toward achieving a viable Ge MOS technology [7,8]. Despite improvements, there are a number of challenges which must be addressed if one aims at developing a viable Ge MOS technology [9]. One of the biggest challenges is to combine high channel mobility with aggressive gate oxide scaling. On the basis of capacitor data, HfO_2 with ultrathin GeON passivating interlayers are promising to achieve sub-1 nm EOT [10,11]. Recently, Ge p-FETs with molecular beam deposited (MBD) $GeON/HfO_2$ gates have been demonstrated which show EOT much less than 1 nm [12] and remarkably high I_{ON}/I_{OFF} ratio $\sim 10^5$ [13]. However, channel mobility and dc performance characteristics are not as good as expected, especially for n-FETs. Although GeON interlayer is necessary to obtain functional devices, it does not provide sufficient passivation of Ge interface [14,15]. This is evident from the CV characteristics [15] which are far from ideal showing large hysterisis, stretch-out and strong frequency dispersion in all regions from accumulation to inversion [16]. In addition, interface state density D_{it} is rather high, in the order $\sim 10^{13}$ eV^{-1} cm^{-2} and cannot be cured by hydrogen annealing or other post deposition treatments. Another problem is that the interfacial GeON layer deposited by MBD is often unstable and, in the presence of HfO_2, is dissociated allowing diffusion of Ge [17] or GeO_x [18] complexes inside HfO_2.

Because of all the aforementioned problems, the general consensus is that alternative passivating materials and high-k oxides are needed. We have recently found [15,19,20] that rare earth oxides and CeO_2 in particular are "friendly" with Ge. They can be deposited directly

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on Ge without the need of interfacial layers, producing improved electrical characteristics with reduced D_{it}. However, due to its small energy gap [21], CeO_2 is leaky [19] and cannot serve as a gate dielectric unless it is combined with other oxides, e.g. HfO_2, to provide sufficient insulation. It is not known however whether the two oxides are compatible and that they can withstand transistor wet processing conditions especially considering that CeO_2 is slightly hygroscopic, as are most of the rare earth oxides.

In the present work we first study the dielectric properties of CeO_2 in terms of generic MIS capacitors. Subsequently, we evaluate the candidate gate CeO_2/HfO_2 materials combination at the highest possible level showing that etched-gate MOS capacitors and functional p- and n-FETs can be made. The p-FETs exhibit exceptionally high I_{ON}/I_{OFF} ratio $\sim 10^6$ and decent channel mobility and dc characteristics, comparable to those obtained in more "standard" $GeON/HfO_2$ devices.

2. Deposition of gate dielectric stack

The gate dielectric stack was prepared by oxide molecular beam deposition (MBD) on bulk n- and p-type Ge(1 0 0) substrates with a resistivity of $\rho \sim 0.02\,\Omega\,cm$. The native oxide was thermally desorbed in situ in UHV conditions by heating the substrate at 400 °C for 15 min until a (2×1) reconstruction pattern was obtained by RHEED, indicative of a clean Ge surface [11,20]. Subsequently, CeO_2 and HfO_2 were sequentially deposited at 225 °C by evaporating Ce and Hf from e-beam sources in the presence of atomic oxygen generated from a remote RF plasma source. The atomic oxygen promotes oxidation at low temperature and low O_2 partial pressure of about $2–4\times 10^{-6}$ Torr used in this work. A number of CeO_2 samples were used to study the dielectric properties of Ceria in terms of generic MIS capacitors as described in Section 3 below. An other set of samples with the bilayer CeO_2/HfO_2 gate dielectric structure was used for the fabrication of MOSCAPs and FETs as described in Section 4. Structure details, nominal thickness and CET values are given in Table 1, Section 4.

3. Dielectric properties of Ceria

Our previous studies [9] of the electrical parameters of Ceria on Ge as a function of growth temperature T_g in the range between room temperature and 360 °C showed a mixed behaviour. As the temperature increases, D_{it} and gate leakage are improved but EOT is degraded. This is consistent with the presence of a low-k interfacial layer and it is further supported by TEM/EELS [15,22], which show that a Ce–O–Ge interfacial layer (IL) is spontaneously formed during the growth. ToF-SIMS also shows [15] that the IL becomes thicker at higher T_g. An optimum temperature of 225 °C is chosen in this work for further studies of the dielectric properties of Ceria.

Several samples with different CeO_2 thickness from 8 to 17 nm were prepared on n and p-type substrates and subsequently characterized electrically using generic MIS capacitors. These devices were made by e-beam evaporation of Pt using shadow masks. Eutectic In-Ga alloy was used as the back ohmic contact. The high frequency (1 MHz) $C–V$ results are shown in Figs. 1 and 2 for as-deposited capacitors made on p-type and n-type Ge, respectively.

The curves were fitted using our model [23] which takes into account quantum corrections by solving self-consistently Poisson's and Schroedinger equations. From the fitting, EOT values were obtained and plotted as a function of the physical thickness t in Fig. 3. From the linear fitting and assuming that Eq. (1) is a good approximation, the dielectric constant of Ceria can be estimated from the slope to be $\kappa_{Ceria} \sim 23$ (± 2).

$$EOT = t_{IL}^{eq} + (k_{SiO_2}/k_{Ceria}) \times t \quad (1)$$

The equivalent IL thickness is estimated from the interception with the y-axis to be $t_{IL}^{eq} \sim 9.1(\pm 1.6)$Å. Taking into account that for thick samples the physical thickness of the IL is about 25 Å [15], it can be inferred that the dielectric constant of the IL is about 11.

The presence of a low-κ interfacial layer combined with the high leakage current [15,20] (see also data and discussion in Section 5.1) is a concern for CeO_2 scaling. This indicates that CeO_2 cannot stand alone as a gate dielectric and needs to be combined with another material, such as

Table 1
Gate dielectric stack parameters

Sample ID		CET (nm)			Gate dielectric stack
p-Ge	n-Ge	A-type	B-type	C-type	
1		1.68	1.72	1.95	9 nm CeO_2
	5	2.37	2.33	2.65	
2		Unable to measure CET			0.6 nm CeO_2/4 nm HfO_2
	6	1.91	2.07	2.19	
3		Broken in Shipment			1.5 nm CeO_2/4 nm HfO_2
	7	2.70	2.60	Broken	
4		2.25	2.24	2.35	1.5 nm CeO_2/3 nm HfO_2
	8	2.52	2.43	2.78	

Types A–C correspond to different thermal treatments.