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Innovating SOI memory devices based on floating-body effects

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Abstract

Scaling considerations of conventional DRAMs lead to recent developments of capacitor-less, single-transistor (1T) DRAM based on the floating-body effects in SOI transistors. Several options (Z-RAM and TTRAM) are reviewed and discussed in terms of operation mechanisms, performance and scaling. We also describe a new concept of 1T-DRAM (named MSDRAM) simple to fabricate, program and read. Its basic mechanism is the meta-stable dip (MSD) hysteresis effect which takes advantage of the coupling between front and back interfaces in SOI transistors. Systematic measurements show that MSDRAMs are suitable for low-power applications as they exhibit negligible off-state current, long retention time and scalability.

Keywords: 1T-DRAM; Capacitor-less; MSD effect; SOI; Floating-body; Memory

1. Introduction

With the increased demand for large-capacity, high-speed, low-power embedded memories, scaling requirements have lead to recent developments of capacitor-less DRAM in SOI technology such as Z-RAM (zero-capacitor RAM) or TTRAM (twin-transistors RAM) [1–5]. In this paper, the architecture, operating principles and main memory advantages of these devices are reviewed and finally compared to our new 1T-MSDRAM (one-transistor MSD-based DRAM) [6,7].

An embedded DRAM, which consists of one-transistor and one-capacitor (1T/1C, Fig. 1a), has a small cell size and a high operation speed. The main issue lies in cell area reduction hampered by the capacitor integration and scaling. For each 1T/1C DRAM memory generation, a constant capacitance value of 30 fF/cell is targeted [8]. At the 100 nm node, this requires a complicated stack or a deep-trench capacitor which leads to additional process steps, lessening the compatibility with standard digital CMOS.

In order to solve this dramatic scaling problem, an alternative solution has been proposed where the conventional storage capacitor is replaced by the thin-film body of a SOI MOSFET. The memory storage mechanism is based on the threshold voltage shift produced by majority carrier excess (accumulation) or deficit (depletion) in the floating-body (Figs. 1b and c). Since there is no body contact to instantly adjust the majority carrier concentration, equilibrium is retrieved only after a relatively 'long' period of time which renders SOI memories attractive in terms of retention and refresh time. Main advantages of capacitor-less memories, compared to conventional DRAM [1], are the cell size reduction and non-destructive reading.

The first capacitor-less 1T-DRAM using standard partially depleted (PD) SOI technology was proposed by Okhonin et al. [1], based on earlier investigations of the transient drain current in SOI MOSFETs [9–14]. The

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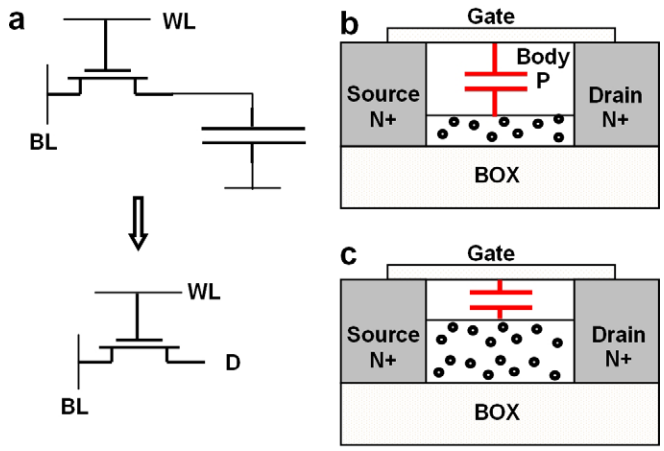

Fig. 1. (a) From conventional one-transistor/one-capacitor (1T/1C) DRAM to one-transistor (1T) capacitor-less DRAM on SOI. (b) In '0'-state the body of the PD transistor is discharged. (c) In '1'-state, excess holes charge the body reducing the depletion region and lowering V_T.

writing (i.e., body charging) of these memories makes use of impact ionization and/or band-to-band tunneling (GIDL) [15].

To ensure the scalability of this new memory named zero-capacitor RAM (Z-RAM), similar operation principles on more advanced devices such as fully depleted (FD) SOI MOSFETs [16,17], double-gate (DG) MOSFETs, and FinFETs were also demonstrated. Recent results were obtained for a Z-RAM cell based on a CMOS Fin-FET, which features vertical multiple independent gates (MIGFET) [3,18,19].

Another type of capacitor-less DRAM using two serial PD SOI MOSFETs was proposed by Morishita et al. [5]: the twin-transistor RAM (TTRAM). This memory cell takes advantage of the coupling between the two transistors to control the storage node potential and consequently the hole charge increase in the body. Although the TTRAM cell needs two transistors, simple array control is achieved as compared with the 1T capacitor-less cell. Therefore, TTRAM features high-speed array operation like the conventional embedded DRAM. In addition, the active power consumption can be also reduced, because the bit-line voltage is lowered to half V_{DD} swing.

Finally, we propose a different single-transistor capacitor-less DRAM which is operated at low drain voltage and enables low-power applications. The basic mechanism is the meta-stable dip (MSD) effect recently discovered [6]. MSD gives rise to an hysteresis in $I_D(V_G)$ curves and a dip in transconductance. We demonstrate by systematic measurements and simulations that MSDRAMs [7] with long retention time can be achieved. The MSDRAM is mainly dedicated to double-gate technology. On the other hand, to document the feasibility of our new memory with advanced technology, 2D numerical simulations were performed for DG-MOSFETs with channel lengths down to 50 nm.

2. Z-RAM

In this section, the basic read and write mechanisms as well as the main device-physics phenomena are introduced. These features are explained for the PD SOI NMOSFET Z-RAM case, but will be next extended to more advanced technologies through scaling considerations.

2.1. Operation principles

The floating-body cell is a standard SOI MOSFET whose drain current I_D is modulated through the charge state of the floating-body constituted by the silicon film. The fundamental memory cell characteristic is a change in threshold voltage between the '0'-state (or low drain current level) and '1'-state (or high current level).

In SOI technology, the threshold voltage strongly depends on the amount of majority carriers charge in the quasi-neutral zone. In the following, only the nMOSFET case will be considered, but same considerations can be applied to the pMOSFET. The majority carriers, i.e., holes, injected into the body produce a substantial body potential increase yielding to a threshold voltage decrease and a drain current enhancement. As the channel length decreases, the drain current level can be further amplified by the parasitic bipolar effect.

The purpose of the Z-RAM programming is thus to modulate the threshold voltage by changing the majority carriers charge in the quasi-neutral zone. To enhance the threshold voltage shift between the '0'- and '1'-states, the holes are, respectively, extracted from or injected into the body (Fig. 1b and c). The resulting current difference can be observed in the $I_D(V_G)$ curves measured just after writing '0' (extraction) or '1' (injection). A large threshold voltage shift is essential for this kind of memory since the '0'- and '1'-states will be determined by current sensing (or sense amplifier). But the key point is the '0'-state retention time, that is, the device capability to maintain the charge deficit in the body.

During '0' write, the majority carriers are extracted from the quasi-neutral zone, for example by applying a negative drain voltage V_D pulse. The body potential decreases below its steady-state value, becoming more negative. The drain- and source-to-body junctions are reverse biased. Consequently, after '0' write, the holes tend to flow from the drain (source) to the body, increasing the potential and the holes charge. This hole leakage current is the critical point of the Z-RAM '0'-state retention time. Nevertheless, the bias conditions used during reading and holding can help to limit the body charging.

During '1' write, the majority carriers are initially injected, from drain or pinch-off region, towards the quasi-neutral zone (e.g. by applying a positive drain voltage V_D). The body potential increases and the source/body junction can be forward biased. Just after '1' write, a few extra majority carriers are sufficient to increase considerably the drain current, but they can also escape from the