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Reconfigurable threshold logic gates with nanoscale DG-MOSFETs

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Abstract

The benefits in using double-gate (DG) MOSFETs as components of threshold logic gates (TLG) have been analyzed for the first time. A novel, variable-weight DG-TLG has also been proposed, which can greatly widen the range of reconfigurable functions accessible to users. Both fixed and variable-weight DG-TLG circuits operate correctly at a low supply voltage of 1.0 V, and outperform the conventional CMOS equivalents in terms of the most important metrics such as power, speed and area. It is found that variable-weight DG-TLG circuits with analog weight and threshold control have attractive features such as expanded TLG functionality, reduced transistor count, low programming voltages and power-scaling capability, particularly for circuits with four or fewer inputs.

Keywords: Threshold logic; Double-gate MOSFETs; SOI; Reconfigurable logic systems

1. Introduction

The double-gate (DG) MOSFET has been proposed as an effective solution to CMOS scaling concerns below 45 nm node [1,2]. As with any new device architecture, DG architecture might be expected to have benefits and disadvantages peripheral to the reason for their introduction. For instance, the possibility of separately driving the gates of a DG-MOSFET (i.e. dynamic threshold control of one gate using the other) may have advantages in reconfigurable logic architectures [3–5]. Yet, it is also important to analyze whether the functional advantages outweigh the loss of intrinsic device performance in such an independently-driven DG-MOSFET (IDDG) as compared to the symmetric counterpart (SDDG). In the present paper, not only do we explore novel reconfigurable circuits using DG-MOSFETs in the context of threshold logic gates, but also indirectly address this basic question (i.e. performance *versus* functionality in DG architecture).

In order to build reconfigurable logic systems, we propose a novel implementation of universal threshold logic gates (TLG) [6] based on DG-MOSFETs, which have never been proposed nor investigated before. TLG are lesser-known but more powerful logic gates that can implement not only basic Boolean gates, but also more complicated multiple-input gates such as 'minority' or 'majority' functions all by setting of an evaluation threshold (T) behind a summing block ($\Sigma w_i x_i$). In other words, they are multi-state logic systems internally with a binary output:

$$\begin{aligned} F &= 0 \quad \text{if} \sum w_i x_i < T \\ F &= 1 \quad \text{if} \sum w_i x_i \geqslant T \end{aligned} \tag{1}$$

where w_i are the weight element for the ith input x_i. For instance, a three-input threshold gate with $w_1 = w_2 = w_3 = 1$ functions as an AND gate for $\mathbf{T} = 3$, an OR gate for $\mathbf{T} = 1$, and MAJORITY gate for $\mathbf{T} = 2$. Because a TLG is able to compare a user set threshold against weighted inputs ($w_1 x_1$), it can also be used to build neural networks, thus having very significant application potential besides

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traditional logic applications. Clearly, the ability to reconfigure logic functionality itself is a very desirable feature, especially in applications where adaptive systems are required or operational limitations (power, size etc.) exist. Although several works that utilizes DG-MOSFETs in reconfigurable applications have been published so far [2,4,5,7], the tunability of the DG-MOSFETs have not been utilized in the context of TLG.

In present work, beyond a simple substitution of DG-MOSFETs in the previously suggested circuits [6,8], we also introduce a novel topology with programmable weight and reduced transistor count. Weight programming provides an additional flexibility in TLG design and expands the reconfigurable function space in a dramatic fashion. We outline below the basic features of this new DG-TLG architecture, verify its feasibility and explore its performance.

2. DG-MOSFET devices and modeling

In an effort to improve the command of the gate over the channel potential, a DG-MOSFET utilizes an additional gate below its ultra-thin silicon body, thus leading to significant improvement in current drive and short-channel performance, as recognized by the Silicon Roadmap [1,9]. Another particularly attractive feature of DG-MOSFET is its capability of tuning the front gate functionality via bottom gate bias when they are independently driven [4,5]. This has a number of important implications for circuit design: (i) increased functionality for a given number of devices; and (ii) reduced parasitics and layout area for equivalent functionality, (iii) higher-speed operation and lower-power consumption with respect to equivalent conventional circuits.

The generic DG-MOSFETs (see Fig. 1a) considered in this work have $t_{Si} = 10$ nm, $t_{ox} = 2$ nm and $L = 100$ nm, where the I_{ON}/I_{OFF} ratio is maximized, delay · power product is minimized and both gates have been optimized for $V_T = \pm 0.25$ V using a dual-metal process [10]. The threshold control via back-gate bias is illustrated in I–V curves of Fig. 1b, where the drain current is studied as a function of front gate bias. The resulting independently-driven devices (IDDG) are always inferior to symmetrically driven counterparts (SDDG) in terms of transconductance and subthreshold performance, under equal geometry and bias conditions. This is because the current increases more than twice in SDDG configuration as compared to IDDG as a result of firm electrostatic coupling between the two gates across the *thin* Si body. Thus bottom gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price that may be justified by increased functionality, as explored below.

The transient and DC response of DG-TLG circuits are obtained using ISE TCAD device simulator Dessis [11] in drift-diffusion approximation without quantum mechanical corrections. These simplifications were necessary in order to reduce simulation time to manageable levels, as each DG-MOSFET contained ~2000 mesh points. While undesirable, the use of such a simplistic transport model and the omission of quantum mechanical corrections are reasonable as we wish to capture first-order effects at this preliminary study. In any case, they will primarily affect the threshold voltage of devices without major implications for circuit functionality or our conclusions.

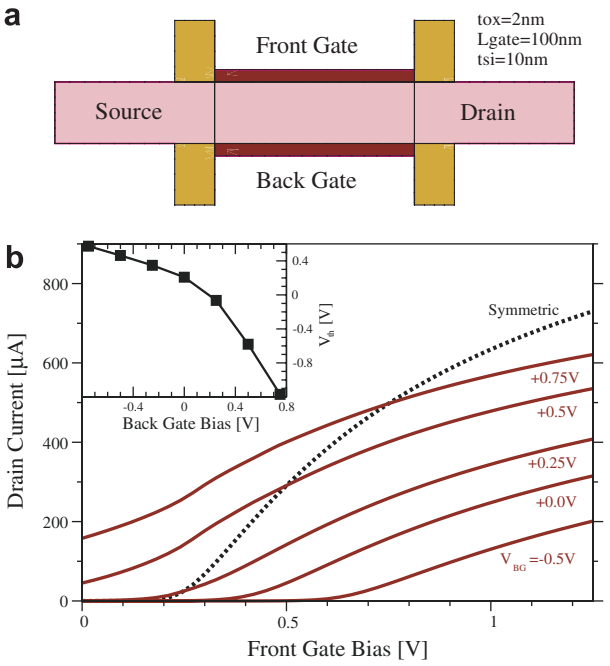

Fig. 1. (a) The generic DG-MOSFET device structure used in this work has a gate length $L_g = 100$ nm, a body thickness $t_{Si} = 10$ nm and oxide thickness $t_{ox} = 2$ nm, typical values for digital applications, and (b) $I_D - V_{FG}$ characteristics of an n-type DG-MOSFET at different back-gate bias conditions. For comparison symmetric ($V_{bg} = V_{fg}$) drive case is also included. Inset shows the extracted front gate threshold voltage (Vth) as a function of back-gate bias.

3. DG-TLG with fixed weight

One of the simplest approaches to building and programming a TLG is to choose an identical number of transistors at the input and threshold (reference) block. It is also desirable to employ a clocked-latch comparator so that power dissipation is minimized [8]. As can be seen from Fig. 2, the resulting DG-TLG circuit requires two binary vectors $[x_i]$ and $[T_i]$ to be applied to activate any number of inputs and reference transistors needed. For this approach to work, both the input (M_{si}) and threshold transistors (M_{ti}) must be equally sized. An additional half-sized transistor (M_{sx}) with a grounded bottom gate is required on the input side to deal with case of $I_{sum} = I_{ref}$, where $F = 1$ is expected. Moreover, it is important to set one of the gates of M_{t1} and use the other gate as LSB of T_i (i.e. T_1) so that $I_{sum} \neq I_{ref}$, even when the electrostatic coupling between the two gates leads to a super-linear (~2.5×, see Fig. 6a later) increase in drain current. In principle, one may choose $1.5 > (W/L)_{sx} \geqslant 1$ to be safe with regard to the current increase in the symmetric mode of operation.