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Design and simulation of integrated inductors on porous silicon in CMOS-compatible processes

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Abstract

We present a comprehensive approach of designing on-chip inductors using a CMOS-compatible technology on a porous silicon substrate. On-chip inductors realized on standard CMOS technology on bulk silicon suffer from mediocre *Q*-factor values partly because of the loss created by the Si substrate at higher frequencies, in addition to the metal losses. We examine the alternative of using porous Si as a thick layer isolating the Si substrate from the metallization in an otherwise standard CMOS technology. We present theoretical designs produced with full-wave Method-of-Moments simulations, verified by measurements in standard 0.18 μm CMOS technology using Al metallization. When porous Si is introduced in that technology, the same inductor metallization produced *Q*-factor enhancements of the order of 50%, compared to the same inductor on bulk crystalline silicon. We also produce optimized single-ended inductor designs using Cu on porous Si, in a 0.13 μm-compatible CMOS technology. The resulting *Q*-factors are enhanced by a factor of 2 and reach values of 30 or more in the 2–3 GHz frequency range. Even higher quality factors can be obtained in this technology when differential designs are used.

Keywords: CMOS on-chip inductors; Porous silicon RF isolation; Quality factors; RF device

1. Introduction

Radiofrequency (RF) components such as inductors, capacitors, transformers and other resonators, integrated on-chip, are essential building blocks of all analog radiofrequency integrated circuits (RFICs) and their performance at current and future CMOS processes is a major bottleneck to successful system integration, especially for single-chip radios at high frequencies [1–4]. This bottleneck prevents a larger-scale integration of analog stages, essential for wireless communication chips, most notably of filters, which currently remain off-chip. Part of the problem relates to metal and substrate losses, inherent to the silicon substrate and other materials and processes currently used in standard CMOS technology, while another part is the inadequacy of lumped-element design rules to correctly account for fully-electromagnetic physical effects at high frequencies. At frequencies of 5 GHz and higher, CMOS integration density at the 90 or 65 nm technology nodes severely violates ideal design rules due to the underlying loss mechanisms of the Si substrate. Integration of RF components and most notably RF inductors, on silicon, suffers from mediocre quality factors [3,4] imposed by both technology characteristics and die area restrictions. It is clear that fully on-chip inductors in a CMOS-compatible process improving the current art by perhaps a factor of 2 could create a significant competitive advantage in the overall performance/cost ratio compared to the hybrid technologies. An important step towards the implementation of improved RF inductors on a standard CMOS technology is the use

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of porous silicon as a compact micro-plate with low RF losses, grown locally on the silicon substrate by electrochemistry. Very thick porous Si layers can be fabricated on the silicon substrate without severe stress problems, as those encountered in conventional microelectronic dielectrics such as silicon dioxide or silicon nitride. Relative dielectric constants of porous silicon are adjustable from below 3 to 9 by changing the porosity of the material from 80% to 25% [5,6]. Porous silicon with more than 50% porosity has low loss tangent (below 10^{-3}) at 20 GHz [7], demonstrating its superiority in RF ranges, compared to bulk crystalline silicon.

In this paper, the use of porous silicon isolation technology in combination with a standard CMOS technology will be assessed by first developing insulator designs, simulation and verification on 0.18 μm CMOS technology and then extracting by simulation the inductor characteristics when the silicon substrate is replaced by a porous silicon layer of a given thickness, dielectric constant and loss tangent.

2. Full-wave Method-of-Moments simulations, inductor designs and verification on 0.18 μm CMOS technology

In this section we will present the performance of an optimized on-chip inductor design realized in 0.18 μm CMOS. We have used the widest metal trace allowable by foundries (typically 35 μm), and standard metal thicknesses. All metal layers are aluminum. A 6-metal 0.18 μm CMOS can have a 2 μm-thick top layer (M6) and this is the version we will be using. For simplicity, we will use single-ended designs where the inductor has two ports: Port 1 is used to inject RF power while Port 2 is used either as output or as ground. In the first case the inductor is used in series by a single signal, while in the latter case it is used as a shunt element, or as an RF choke etc. In the rest of this paper we will consider the second port of the inductor as grounded.

Another important topology of on-chip inductors is that of differential inductors [8], whereby the two inductor ports are fed by a differential RF signal. This configuration allows for somewhat higher Q-factors (for the same inductor sizes) but changes in the underlying foundry technology affect optimized designs in this class similarly to the optimized single-ended inductors, therefore, we will not discuss differential inductors further.

The simplest possible characterization of a single-ended inductor, is shown in Fig. 1. In Fig. 1(a) we show the 2-port circuit while in Fig. 1(b) we show the 1-port circuit (with the second port grounded). We will consider port 1 to always be the top populated metal of the structure, which turns out to be the configuration producing the highest Q, while the port closest to the substrate is grounded. For this configuration, the inductance L is found as the DC limit of the inductive function $L(\omega)$,

$$L(\omega) \equiv \mathrm{Im}\left[\frac{1}{\omega(Y_{11}(\omega))}\right] \quad L = \lim_{\omega\to 0} L(\omega) \tag{1}$$

where $Y_{11}(\omega)$ is the device's complex admittance at port 1 (found from full-wave electromagnetic simulations or measurements), the angular frequency $\omega \equiv 2\pi f$ and f is the frequency. To calculate the Q-factor at any frequency we solve the circuit of Fig. 1(b) through the identity

$$Y_{11}(\omega) = \{Y_{11}(\omega)\}_{\text{circuit}}. \tag{2}$$

This produces a series resistance and a shunt capacitance that are both functions of the fitting frequency, i.e., $R(\omega)$ and $C_1(\omega)$. The Q-factor of the device can be calculated by the formula at resonance as

$$Q(\omega) = \frac{\omega L}{R(\omega)}. \tag{3}$$

Eq. (2) is an algebraic system of two equations with two real unknowns. Its solution provides the quality function of Eq. (3) in closed form as

$$Q(\omega) = Q_0(\omega) + \sqrt{Q_0^2(\omega) - 1} \quad \text{with}$$
$$Q_0(\omega) = \frac{1}{2\omega L \mathrm{Re}\{Y_{11}(\omega)\}}. \tag{4}$$

The capacitance is similarly found to be

$$C_1(\omega) = \frac{\mathrm{Im}\{Y_{11}(\omega)\}}{\omega} + Q(\omega)\frac{\mathrm{Re}\{Y_{11}(\omega)\}}{\omega}. \tag{5}$$

While these formulas produce frequency-dependent element values and hence do not provide a correct broadband circuit model for the device, (i.e., a circuit valid for all frequencies), they do provide the correct characterization for the inductance and for the Q-factor. Indeed, Eq. (1) provides the inductance L as the DC limit of the inductive function $L(\omega)$ and therefore L is a frequency-independent constant. Eq. (4), on the other hand, is a closed-form solution for the Q-factor that can be used directly with electromagnetic simulations or measurements. We note, however, that broadband circuits with constant element values can be produced, and are important for multi-stage interconnection (see, for example, [9]).

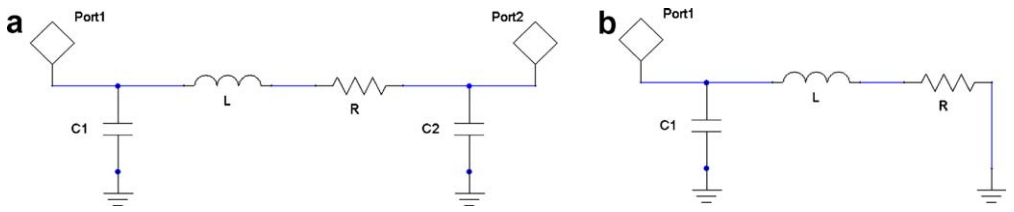

Fig. 1. (a) 2-Port circuit model and (b) the resulting 1-port circuit model for calculating a closed-form formula for the Q-function of the inductor.