Sensors and Actuators A 150 (2009) 237–242

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

Study of symmetric microstructures for CMOS multilayer residual stress

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ARTICLE INFO

Article history:
Received 10 June 2008
Received in revised form 13 January 2009
Accepted 15 January 2009
Available online 23 February 2009

Keywords:
CMOS–MEMS
Residual stresses
Symmetric multilayer flat-plane
Isotropic etching

ABSTRACT

This study presents a fabrication-based approach to improve the curl-up effect in complementary metal oxide semiconductor (CMOS) multilayer large-area planar structures. Control of the residual stress of CMOS multilayer microstructures is necessary for development of microelectromechanical systems (MEMS) sensors such as accelerometers and micromirrors. In this work, 3D symmetric geometry can be used to overcome effectively the residual stresses in CMOS multilayer microstructures. To demonstrate this concept, a symmetric multilayer flat-plane is fabricated and release-etched using an isotropic plasma etching process. The isotropic etch characteristics and lateral undercut can be controlled using a chamber pressure of 0.47 ± 0.2 Torr. A flat-plane structure with an area of $500\,\mu m \times 500\,\mu m$ is fabricated using multilayer materials, including four metal and three silicon dioxide layers. Based on this approach, the measured results show the residual stress effect can be minimized in CMOS multilayer microstructures, and furthermore the curl-up effect of flat-plane is less than $2\,\mu m$ across the $500\,\mu m \times 500\,\mu m$ area.

1. Introduction

In the last decade, the development of microelectromechanical systems (MEMS) devices using standard complementary metal oxide semiconductor (CMOS) processes has been markedly accelerated by leveraging mature manufacturing technologies from the semiconductor industry. Pressure sensors [1], microphone [2], gas sensors [3], accelerometers [4], resonators [5], micromirrors [6], and biosensors [7] have all been designed, fabricated, and reported in the literature. Recently, MEMS sensors have gained much attention because of their wide range of applications, due to their advantages of low cost, low weight, low power and high quality [8–10]. However, the production of low cost MEMS products requires monolithic integration and compatibility with CMOS technology. One of the important issues for CMOS–MEMS devices is residual stress. It can affect the mechanical properties and long-term electrical performance of sensors [11,12]. The residual stress is not constant, and usually depend on experimental and environmental factors such as fabrication, temperature, pressure and time [13,14].

In general, the materials in multilayer CMOS process technology used in foundries include silicon, polysilicon, interlayer dielectrics, and metal interconnects. Each of these materials can become MEMS structural materials. The difference among the coefficients of thermal expansion of the multilayers can create complicated residual stresses in the finished CMOS–MEMS device. At present, various means to minimize the residual stress in standard CMOS processes have been reported [15,16]. In order to enhance the performance of CMOS–MEMS devices, lower stress materials and thicker layers can be considered. For example, a CMOS–MEMS gyroscope used a thicker commercial copper (Cu) composite material [15]. In this research, the Cu metal material was used in a low-temperature CMOS process, to influence the mechanical strength and thermal properties and generate lower stress in the fabricated devices. Moreover, the authors have shown structures (utilizing six Cu-based and six dielectric-based layers) that is thicker than one aluminum (Al) metal material. Specifically, the 12-layer stack thickness is $8\,\mu m$, versus $5\,\mu m$ for a conventional Al approach. However, Cu has higher activity than Al. It diffuses more easily into silicon and contaminates silicon-based devices. Additionally, Cu-based CMOS processing is more expensive than Al-based processing. As another example, thicker microstructures of CMOS–MEMS micromirrors were obtained using deep dry etching process with a high aspect ratio [16]. In this research, deep dry etching is employed to make a thicker single-crystal silicon layer to reduce the effect of the residual stress in CMOS multilayer microstructures. Based on this approach, fabrication required an expensive, high-precision, double-side alignment lithography tool.

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0924-4247/$ – see front matter.
doi:10.1016/j.sna.2009.01.012

This study focuses mainly on fabricating large-area multilayer flat-plane structures using an isotropic etching process. This novel approach uses symmetric geometry in the vertical direction to decrease the effect of CMOS–MEMS residual stress. Symmetric flat-plane microstructures are fabricated using the TSMC 0.35 μm 2P4M CMOS–MEMS process [19]. Flat-plane structures with a size of 500 μm × 500 μm comprise four metal layers and three silicon dioxides layers. The measured results demonstrate that the planar curl-up effect is minimized using this fabrication process.

2. Fabrication principle for CMOS multilayer residual stress

This study attempts to balance and minimize residual stress of CMOS multilayer microstructures by using symmetric structures. The distinction between symmetric and non-symmetric CMOS microstructures hinges on whether the materials are present under the bottom metal layer, as shown in Fig. 1. CMOS symmetric structures are employed to introduce a new approach for releasing these materials. Wet and dry conventional etching are employed [13,17]. Although wet etching has a higher etching rate and better selectivity, the surface tension of the etching solution between the released structures and the substrate causes stiction phenomenon in the micro/nano-fabrication [13,18]. Stiction during the release of the structure can be avoided by dry etching approaches. Table 1 shows three dry etching techniques—sputter etching, plasma etching and reactive ion etching (RIE) [13,17]. Table 1(a) and (b) present the anisotropic etching process. Table 1(c) shows an isotropic plasma etching process that differs from that in Table 1(a) or (b).

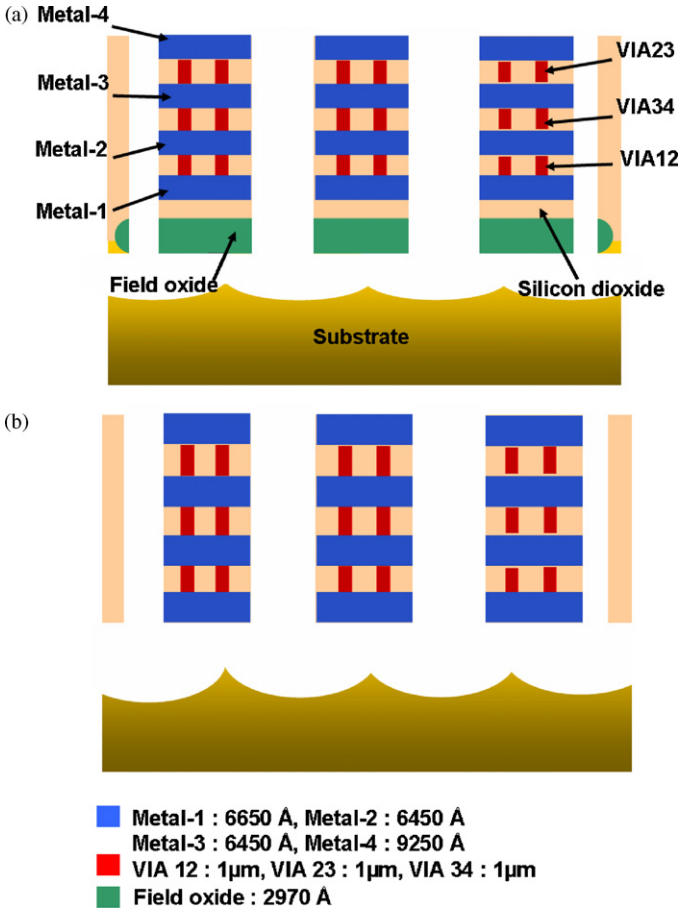

Fig. 1. Schematic cross-section view after standard CMOS process. Schematic illustrations of the conventional and novel CMOS multilayer studies are (a) non-symmetric and (b) symmetric microstructures, respectively. The ideal symmetric microstructures of CMOS devices have no material under the metal-1 layer. This design and fabrication is a novel concept of reduction curl-up effect in CMOS multilayer microstructures.

Table 1
Comparison of three types of etching methods in the microfabrication process. Plasma etching has higher selectivity and isotropic etching profile that is very suitable to fabricate symmetric CMOS microstructures.

Type of etching	Pressure (mtorr)	Methods	Selectivity	Geometry
Sputter etching (a)	~10	Physical	Low	Anisotropic
Reactive ion etching (b)	10~100	Physical & chemical	Medium	Anisotropic
Plasma etching (c)	>100	Chemical	High	Isotropic

The post-CMOS process generally utilizes RIE to release microstructures. The RIE system combines plasma etching and ion beam etching. Although similar to a plasma system, this system can still perform ion milling. The major advantage of the RIE system is that it fabricates a high aspect ratio microstructure with an anisotropic feature. Nevertheless, anisotropic etching cannot remove the materials under the etching mask (metal layer), producing non-symmetric microstructures in the post-CMOS process, as shown in Fig. 1(a). Plasma etching is a chemical etching process that yields an etching profile with isotropic characteristics and lateral undercuts. Thus, symmetric microstructures can be fabricated by the plasma etching approach, as shown in Fig. 1(b). Yet, this fabrication approach has received little attention. Although dry etching has been extensively studied, little consensus exists on how symmetric CMOS multilayer large-area planes can be fabricated by isotropic plasma etching.

3. Simulation for CMOS multilayer

Simulation of the complex curl-up of post-CMOS multilayer microstructures can be performed based on finite element analysis (FEA) using the IntelliSuite software (IntelliSense Corp., USA). The simulation involves 10,000 grid cells. FEA modeling of CMOS–MEMS is applied to Al metal, silicon dioxide, field oxide and polysilicon layers, to predict effectively the residual stresses of non-symmetric and symmetric microstructures.

In a CMOS–MEMS device, the choice of the materials depends on the device layout. For example, CMOS accelerometers and gyroscopes require a larger proof mass to increase sensitivity. A thick microstructure with a larger area can be used to fabricate this proof mass [4,15]. Most CMOS–MEMS devices include all layers except a polysilicon layer, because a polysilicon layer has a larger residual stress than other layers [26]. Simultaneously, a polysilicon layer would cause a serious curl-up effect in the CMOS–MEMS device. Thus, in this study, the FEA model of the CMOS–MEMS device includes no polysilicon layer.

In this simulation of large-area CMOS multilayer microstructures, Al, silicon dioxide and field oxide must be considered. The material properties in the simulation are taken from the National Chip Implementation Center [27]. The Young's modulus of Al metal, silicon dioxide and field oxide are 70, 72 and 74 GPa, respectively. Their Poisson's ratios are 0.30, 0.17 and 0.175, respectively [22–24,27]. Fig. 1 presents the thicknesses of each layer.