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Implementation of a scalable VBIC model for SiGe:C HBTs

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Abstract

This work examines the utility of semi-physical vertical bipolar inter-company (VBIC) model for the first time to develop for an accurate, easy and fast scaling methodology for high-frequency SiGe:C heterojunction bipolar transistors (HBTs) with a peak f_T of 75 GHz fabricated in a low-cost BiCMOS technology. The methodology allows one to find transistor models from single-finger transistor to multi-finger and variable length emitter devices with a minimal parameter extraction procedure. The devices modeled include several base–emitter structures in parallel, on top of a single collector to obtain different transistor area. The scaling rules are given in detail. Using this methodology, scalable VBIC model parameters were generated to describe the DC and RF behavior of SiGe:C HBTs up to peak f_T and f_{max} within ±10% accuracy. The key advantage of this methodology is that one does not need any special test structure while keeping the extraction procedure simple and fast.

Keywords: Scalable compact model; VBIC; SiGe:C; HBTs

1. Introduction

Circuit designers need a large range of transistor sizes for different circuit applications. To serve them reliably and effectively through design kits, generation of model parameters quickly and accurately for all the transistor sizes fabricated in a new technology is of great importance and this is commonly known as the scalable model development. Unlike the MOS transistors, which can be considered as a surface device, the bipolar transistors need to be treated along with their three-dimensional effects. Hence, it is difficult and in general, more complex to develop a scalable bipolar transistors model.

The scalability issues in bipolar compact model have been studied and scalable SPICE Gummel Poon (SGP) model has been reported in Refs. [1,2]. Currently, investigations are being carried out to develop laterally scalable high-current model (HICUM) models for HBTs [3–5]. Scalable physics- and process-based SGP and HICUM models [6,7], using a special parameter generation program TRADICA [8], have been employed to model the intermodulation distortion characteristics. Scalable transistor models using VBIC [9], and scalable most excusite transistor model (MEXTRAM) [10,11] are also in the development stage. Most of the studies hitherto carried out, requires either, formulating complex model equations to incorporate geometrical dimensions together with process specific parameters as factors, or to extract electrical parameters simultaneously with the geometric parameters such as area or perimeter dependency for each transistor.

In this paper, we present a simple but accurate scaling methodology using VBIC model for SiGe:C-HBTs, fabricated in a flexible, low-cost BiCMOS technology [12]. One may find some interesting results in Ref. [13] based on an approach partially similar to one developed here. The main aim of this work is to develop a scaling strategy

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for a wide range of transistor sizes with a minimal parameter extraction procedure. The developed scalable model is incorporated into a design-kit allowing one to vary the emitter length and the number of emitter stripes to get a wide range of transistor sizes.

2. Technology and transistor geometries

The detail of the BiCMOS technology, involved in the present study, may be found in Ref. [12]. Briefly, the process involved a minimized thermal impact on the CMOS flow. One goal of this integrated approach is to utilize CMOS process steps in the HBT module. The HBT module offers three devices with $f_T/f_{max}/BV_{CE0}$ values of 28 GHz/67 GHz/7.5 V (high voltage); 52 GHz/98 GHz/3.8 V (standard); and 75 GHz/90 GHz/2.4 V (performance) [12]. In the next section, where scalable VBIC model is presented, all measured and simulated data correspond to the high-frequency "performance" transistors (75 GHz/90 GHz/2.4 V). A Schematic diagram of a "performance" transistor is shown in Fig. 1.

To achieve high performance at a low cost, three-dimensional effects are utilized in the transistor design itself. To reduce the contact resistance, U-shaped collector contact is used whereas the base contact is placed on a shorter edge. Generally, a long emitter leads to the performance degradation due to high base resistance. But for a larger emitter area and consequently a high current, we used a special configuration, layout of which is shown in Fig. 2. It may also be noted that each transistor is shielded with an active ring to avoid influences from the surrounding devices. For high integration, we have put several transistors together. For example, as shown in Fig. 2, if four single transistors of type T1 and equivalent four-emitter transistor of type T3 are compared, almost a 50% area is saved in the latter case. From performance point of view, the emitter length (l_E) is allowed to vary between 0.84 μm and 3.36 μm. Emitter width is constant (0.42 μm) for all the test structures investigated here. To count the number of emitter stripes, two numbers N_x (number of emitters in a row) and N_y (number of emitters in a column) are used. Maximum permitted values for N_x and N_y are 8 and 2, respectively. Therefore, the emitter area (or the corresponding current) can be scaled by roughly a factor of 50 with this scaling approach.

The inner parts of the transistor, i.e., the emitter poly, inner base and collector are independent from each other because of its identical surroundings. So the model parameters related to these regions are easily scalable with N_x and N_y. Below the emitter–base structure, there is a common collector layer, which is formed during the PMOS source/drain implantation in this technology. The product, L_yN_y determines the length of the total collector, where L_y is a function of emitter length (l_E) and L_xN_x determines the collector width, and L_x is a function of emitter width (constant in our test structures). More specifically, the collector area and perimeter is calculated with the layout specific data a, b, and c as shown in Fig. 2. The procedures of scalable model development are discussed in the following sections.

3. Scalable VBIC model

Actual model development starts from generating the scaling equations. Test structures and scaling equations are detailed in Section 3.1. The measurement techniques and the equipments used are discussed in Section 3.2 followed by the results and discussion. At last, a short discussion on the implementation of the scaled model in a design-kit is provided. Software package IC-CAP, from Agilent Technologies inherently linked to Spectre 4.4.6 (incorporating version 1.1.5 of VBIC) from Cadence Design System, was used for the measurement, parameter extraction and simulation. The scaling equations developed were also implemented in IC-CAP parameter extraction language (PEL) along with the parameter extraction procedures.

3.1. Test structures and scaling equations

In the scaling strategy, as pointed out earlier in Section 2, a change in the emitter length and emitter stripe, changes transistor geometry. Emitter length is scaled by a factor of four, while the number of emitter stripes counted by N_xN_y was varied from 1 to 16. All nine test structures used in the present investigation are shown in Fig. 3, in which different points signify test transistors with different emitter lengths and number of emitter stripes. Seven test structures with black solid dots are used for parameter extraction, where as two tests structures with triangles are used for verifica-

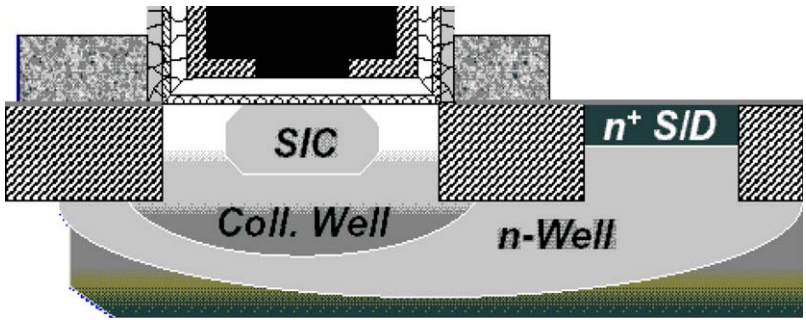

Fig. 1. Schematic of high-frequency performance ($f_T = 75$ GHz) HBTs.