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SCIENCE DIRECT
Solid-State Electronics 50 (2006) 496–499
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Modelling of strained-Si/SiGe NMOS transistors including DC self-heating

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Received 2 December 2005; received in revised form 6 February 2006; accepted 27 February 2006

The review of this paper was arranged by Prof. S. Cristoloveanu

Abstract

In this paper, a new model of surface-channel strained-Si/SiGe NMOSFETs is derived based on the extension of non-quasi-static (NQS) circuit model developed previously for bulk-Si devices. Basic equations of the NQS MOS model have been modified to account for new physical parameters of strained-Si and relaxed-SiGe layers. In addition, the device steady-state self-heating is efficiently included without employing the thermal-flow analog auxiliary sub-circuits. From the comparisons of modelling results with numerical simulations and measurements, it is shown that a modified NQS MOS including steady-state self-heating can accurately predict the DC characteristics of strained-Si/SiGe NMOSFETs.

Keywords: Strained-Si; NMOSFET; Self-heating; Modelling

1. Introduction

Strained-Si (SS) technology is emerging as a leading choice for continuous progression of transistor performances demanded by the International Technology Roadmap for Semiconductors, ITRS [1]. For future circuit applications of these promising devices, the efficient SS MOSFETs models are required. Consequently, there is a strong interest in the extension of conventional bulk Si MOSFET models to SS devices. A few studies on the extensions of the conventional bulk-Si MOSFET models published so far [2–4] have aimed primarily to estimate the implications of SS devices on final circuits performances. However, the validation of these models with experimental SS device data has not been presented. In this paper, a new model of SS NMOSFET is derived based on our recently described non-quasi-static bulk-Si device model (the NQS MOS model [5]). It appears that, owning to a small set of parameters directly related with the device underlining physics, the NQS MOS model [5] can be easily modified to include new physical parameters of strained-Si and relaxed-SiGe layers. Also, it will be shown that the NQS MOS model can be efficiently modified to include steady-state SHEs. A schematic cross-section of an experimental surface-channel SS NMOSFET fabricated on relaxed $Si_{85}Ge_{15}$ is shown in Fig. 1 together with its identical bulk-Si counterpart processed simultaneously on Si substrates. These test devices are used for parameters extraction and model validation. For more detailed description of their design, technology and electrical performances please refer to [6].

2. Modelling the SS NMOSFETs

In order to extend the NQS MOS model [5] of bulk-Si devices on SS NMOSFETs, some of its basic formulas have

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0038-1101/$ - see front matter © 2006 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2006.02.011

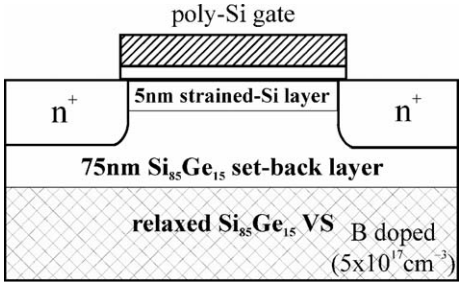

Fig. 1. Schematic cross-section of an experimental surface-channel SS NMOSFET fabricated on relaxed $Si_{85}Ge_{15}$ virtual substrate.

to be upgraded to account for the new physics of SS and SiGe materials. Thus, new intrinsic carrier concentration ($n_{i,SS}$) and relative dielectric constant (ε_{SiGe}) of SS and SiGe layer, respectively, were introduced for calculating the Fermi potential (ϕ_f) and transistor body factor (γ) (see Eqs. (3) and (4) in [5]). Their dependences on Ge mole fraction (x) were taken as

$$n_{i,SS} = n_{i,Si} \cdot \exp(0.4x/2kT) \quad (0 < x < 0.4), \tag{1}$$

$$\varepsilon_{SiGe} = 11.7 + 4.6x. \tag{2}$$

Eq. (1) was derived from the widely accepted semi-empirical SS energy band-gap ($E_{g,SS}$) formula $E_{g,SS} = E_{g,Si} - 0.4x$ [7] and Eq. (2) from the linear extrapolation between Si and Ge relative dielectric constancies, respectively.

The enhancement of low-field electron mobility in the SS layer is described by the new parameter $\mu_{dop,SS}$ that is related with the previous Si mobility parameter ($\mu_{dop,Si}$) by

$$\mu_{dop,SS} = m \cdot \mu_{dop,Si}. \tag{3}$$

The enhancement factor m was determined from the empirical mobility data of SS devices reported in [7], where, for example, $m \approx 1.6$ for $x = 0.15$. Note that, in the case of the n-channel SS MOSFET, a single value of m is found to be a good approximation for both low and high gate voltage V_{GS} [8].

The DC (or steady-state) self-heating effects (SHEs) in MOS devices refer to local increase of channel temperature with dissipating power, that in turn limits maximum device current drive performance [9,10]. In SS MOSFETs, it occurs due to a poor thermal conductivity (at least fifteen times lower than that of Si of the thick SiGe underlayer [11]). The combination of low thermal conductivity and thickness (>1 μm) of the relaxed $Si_{1-x}Ge_x$ layer results in a device structure with low thermal conductance, leading to high SHEs analogous to those often observed in SOI devices with thick buried oxide [9].

The three main SHEs in NMOSFETs are: a decrease of channel mobility, a drop of threshold voltage and an increase of carrier's saturation velocity [9]. In the higher power dissipative region, however, the mobility degradation predominates all other effects, which subsequently appears as a negative conductance in device output characteristics. In widely used SPICE-like method for modelling SHEs [10], the channel temperature (T_{ch}) is assumed to depend on device power dissipation as

$$T_{ch} = T_0 + Z_{th} \cdot (I_{DS} \cdot V_{DS}), \tag{4}$$

where T_0 is the ambient temperature, and Z_{th} is the thermal impedance from the device surface to an external thermal 'ground' contact. For solving Eq. (4), the equivalent circuit is commonly constructed with power being the thermal analog of current and temperature being the thermal analog of voltage [10]. The necessity of extracting device temperature T_{ch} from total power dissipation occurs due to the use of analytical MOSFET models, where T_{ch} appears as an iteratively solved parameter increasing the device model complexity. It often leads to convergence problems in SPICE simulations even for simple circuits. Unlike the analytical MOS models, the drain current I_D of the NQS MOS model is obtained by self-consistently solving the equivalent channel transmission line with pre-determined source/drain boundary potentials [5]. Consequently, SHEs can be incorporated in SS device model not through Eq. (4), where both I_D and V_{DS} are needed, but only through its phenomenological dependence on V_{DS}. Assuming that all SHEs can be summed into one lumped effect of channel mobility degradation, a modified low-field mobility parameter ($\mu^*_{dop,SS}$) is defined as

$$\mu^*_{dop,SS} = \mu_{dop,SS} \cdot (1 - t_1 \cdot V_{DS}^{t_2} \cdot L_{eff}^{-1}), \tag{5}$$

where $\mu_{dop,SS}$ is the original mobility parameter in the NQS MOS model [5], t_1 and t_2 the strain independent fitting parameters, while L_{eff} is the effective channel length. Eq. (5) simply expresses the expected behaviour that, for constant V_{GS}, $\mu^*_{dop,SS}$ tends to decrease with increasing V_{DS} due to thermal effects, and this is especially pronounced in scaled devices since $R_{th} \sim L_{eff}^{-1}$. As the segmental resistance ($R_k(V_{GS})$) of the equivalent transmission line in the NQS MOS model is inversely proportional to $\mu_{dop,SS}$ (see Eq. (A4) in [5]), it yields

$$R_k(V_{GS}, V_{DS}) \propto (\mu^*_{dop,SS})^{-1} \propto (1 - t_1 \cdot V_{DS}^{t_2} \cdot L_{eff}^{-1})^{-1}. \tag{6}$$

An intuitive consideration of the influence of (5) and (6) on simulated DC characteristics can be given as follows. For low V_{GS}, $R_k(V_{GS}, V_{DS})$ acquires very high values in simulations which yield small I_D. Then, a small variation of $R_k(V_{GS}, V_{DS})$ caused by Eq. (6) weakly affects the simulated I_D in the low-power dissipation region (low V_{GS} and low V_{DS}), which complies with experimental findings (please see Fig. 2). However, in strong inversion and for higher V_{GS}, $R_k(V_{GS}, V_{DS})$ becomes very small, and its relative increase with V_{DS} will largely influence calculated I_D values, even for moderate V_{DS} values. When sweeping V_{DS} from low to high values, a negative conductance will appear in simulated I_D–V_{DS} characteristics of SS device as may be confirmed by Fig. 2.