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Short Communication

A novel 50 nm vertical MOSFET with a dielectric pocket

S.K. Jayanarayanan *, S. Dey, J.P. Donnelly, S.K. Banerjee

Microelectronics Research Center, The University of Texas at Austin, Austin, TX 78758, United States

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Abstract

A vertical metal-oxide-semiconductor field-effect transistor with the novel feature of a dielectric pocket between the channel and source/drain has been fabricated and tested. These dielectric pocket vertical MOSFETs (DPV-MOSFETs) show an improved suppression of short-channel effects such as V_T roll-off and drain induced barrier lowering (DIBL). This is due to reduced charge sharing, thus allowing better threshold voltage control. The dielectric pocket also prevents dopant diffusion from the source/drains into the body during device fabrication, mitigating bulk punchthrough.
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Keywords: Vertical MOSFET; Dielectric pocket; Shallow junctions; Short channel effects

1. Introduction

In order to improve the packing density and device performance in ultra-large scale integrated (ULSI) circuits, MOSFETs have been scaled down successfully over the past few decades. However, continued scaling faces challenges such as lithography and short channel effects [1]. Consequently, ultra-shallow source/drain junctions with high conductivity are necessary as the device is scaled down to 50 nm and below [2]. Instead of reducing the junction depth, dielectric pockets that limit dopant diffusion in planar MOSFETs have been proposed and fabricated, and the control of short-channel effects such as V_T roll-off was demonstrated [3]. Vertical MOSFETs offer the possibility of a lithography-independent channel length while reducing the transistor area [4,5]. Fully-depleted vertical MOSFETs that have ultra-thin mesa widths have shown excellent suppression of short channel effects [6]; however, the processing of these MOSFETs requires complex steps such as e-beam lithography and chemical–mechanical planarization (CMP). Recently, a vertical MOSFET with a dielectric pocket to suppress short-channel effects and improve I_{ON}/I_{OFF} ratio has been proposed that requires only conventional lithography and no CMP steps [7]. In the present work, we have fabricated dielectric pocket vertical MOSFETs (DPV-MOSFETs) that show excellent suppression of short-channel effects. The junction depth is easily controlled and the V_T roll-off effect arrested. A reduction in the junction depth results in a reduction of DIBL. The fabrication requires only conventional lithography.

2. Device fabrication

Fig. 1 shows the process flow to realize the DPV-MOSFET device structure. The starting substrate was a (1 0 0) Si 100-mm diameter 0.0015 Ω cm p-type wafer. A 60-nm n-type channel layer was grown by Ultra-high Vacuum Chemical Vapor Deposition (UHVCVD) [8]. A 15-nm oxide layer was grown by wet oxidation at 750 °C for 50 min. A 100-nm polysilicon layer was then deposited

* Corresponding author. Address: One AMD Place, M/S 143, Sunnyvale, CA 94088, United States. Tel.: +1 408 749 4536; fax: +1 408 749 5585.
E-mail address: kartik.j@amd.com (S.K. Jayanarayanan).

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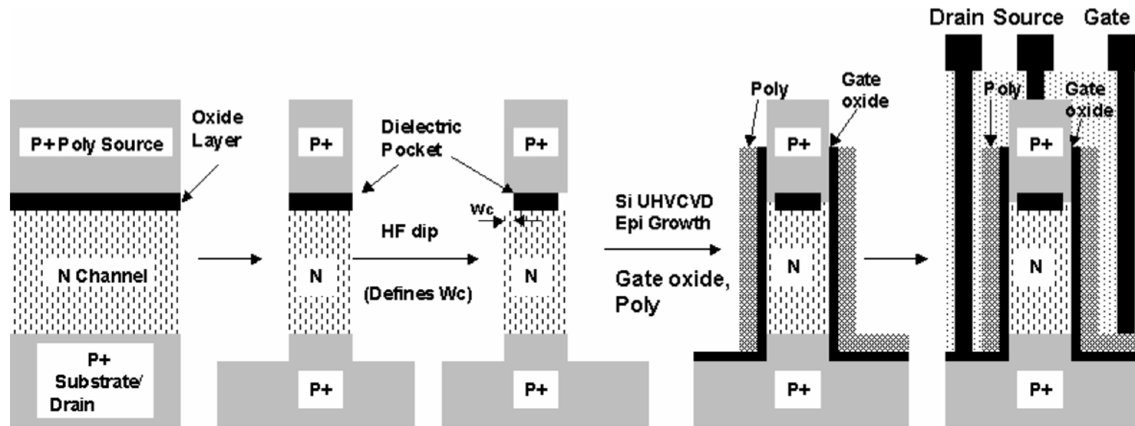

Fig. 1. Process flow for the DPV-MOSFETs.

and doped by BF_2 ion-implantation at 15 keV with a dose of 2×10^{15} cm^{-2}. Subsequently, a reactive ion etch process with HBr and Cl_2 was used to define the mesa of width 20 μm. A timed HF-dip defined the drain contact width (the equivalent of junction depth in planar devices), W_C. A 20-nm silicon epitaxial layer was grown by UHVCVD before growing a 4-nm gate oxide by wet oxidation at 750 °C for 5 min. The relatively thick gate oxide was required due to limitations in the processing furnace. This was followed by 100-nm polysilicon deposition for gate electrode formation. The polysilicon gate was implanted and annealed at 900 °C for 1 min. The rest of the process was a standard MOS process, including low temperature oxide deposition for passivation and contact hole etching, metal deposition and patterning, followed by a forming gas anneal. Secondary ion mass spectroscopy (SIMS) profiles along the channel after processing are shown in Fig. 2. The high channel doping was required due to high levels of background doping in the UHVCVD chamber and is not a requirement of the device. The channel length was determined to be 50 nm from the SIMS profile. This does not take into account diffusion from the source/drain along the vertical wall where there is no dielectric barrier. Simulations show that the diffusion is not more than 10 nm along either side of the channel, so that channel length is definitely more than 30 nm.

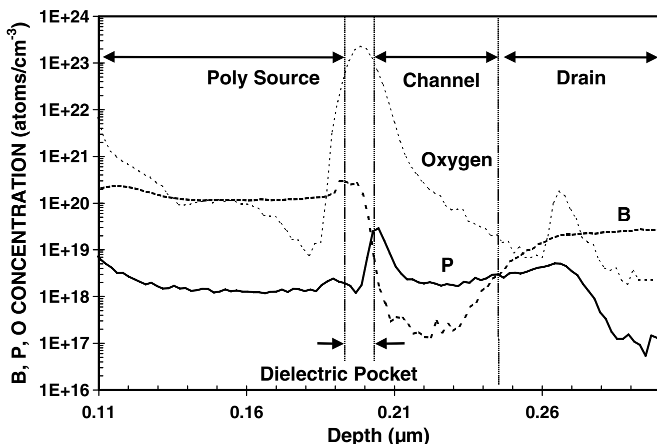

Fig. 2. SIMS profile along the vertical channel.

3. Results and discussion

Simulation studies were undertaken to compare the simulated values of the threshold voltages with the experimental values. Device simulation of the DPV-MOSFET was done using the TAURUS Device Simulator. Drift-diffusion simulations incorporating quantum correction model (for carrier confinement) for different values of the contact width were in general agreement with the experimental results. The simulation parameters were chosen to closely reflect the device fabrication conditions [9].

The dielectric pocket serves a number of functions; it greatly reduces the influence of the large area parasitic bipolar transistor in the vertical structure and also prevents encroachment of the doping from the extrinsic source, thus reducing electrical bulk punch-through effects [10]. Furthermore it reduces charge sharing effects associated with the source and so improves threshold voltage control.

The top P+ polysilicon layer is used as the source in the "normal" mode. In the "reverse mode", the source and drain contacts are interchanged. Fig. 3 shows the subthreshold and output characteristics for the DPV-MOSFET in the normal and reverse modes of operation. The device shows excellent on–off characteristics in the normal mode, but the off-state leakage current in the reverse mode is larger than that in the normal mode. This is due to possible structural defects near the top PN junction in the vicinity of the dielectric pocket, which results in a higher leakage current when reverse-biased. These defects may be removed by Selective Epitaxial Growth of the Si cap layer. The drive current in the normal mode is lower due to the fact that when the source is on top, the source contact width (or junction depth) is lower, which increases the source resistance and decreases the effective gate bias, thereby decreasing the drive current. In the reverse mode, with the source on bottom, there is no increase in source

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