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A thorough study of hydrogen-related gate oxide degradation in deep submicron MOSFET's with deuterium treatment process

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Abstract

Experimental results are presented for gate oxide degradation under direct tunneling stress conditions using p- and n-MOSFET's with gate oxides that are treated with high-pressure hydrogen and deuterium annealing. Device parameter variations as well as the gate leakage current depend on and are improved by high-pressure deuterium annealing, compared to corresponding hydrogen annealing. The precursor for oxide trap is probably created in the bulk of the gate oxide, which depends on hydrogen concentration levels, however its generation is not related with SiO_2/Si interface reaction that produces the released hydrogen. The treatment with deuterium instead of hydrogen in device fabrication provides a possible solution to reduce the generation of oxide-trap precursor within the gate oxide.

Keywords: Deuterium; Gate oxide; Oxide-trap precursor; Hydrogen

1. Introduction

The thickness of gate oxides is currently aggressively reduced to achieve simultaneously high speed and low power circuit operation. To meet all requirements for this regime of operation in advanced CMOS technology, the electric field applied to the gate oxide continues to increase, thus raising reliability concerns for submicron MOS devices. The low-field gate oxide leakage current, following high-field stressing of thin gate oxides, has also been identified as a scaling limitation for non-volatile-memory tunnel oxides. In several investigations, deuterium has been incorporated at the Si–SiO_2 interface by substituting deuterium gas for forming gas during post-metallization annealing under atmospheric pressure [1–4]. The deuterium isotope effect is known to significantly improve gate oxide reliability under hot carrier injection conditions [2,5] and the endurance characteristics of memory devices [6]. The isotope effect is based on a much slower desorption rate of deuterium atoms from the Si/SiO_2 interface. It has also been reported that no isotope effect is observed for the stress-induced leakage current (SILC) under Fowler–Nordheim (F–N) stress conditions, and it was suggested that a model (for gate oxide breakdown) which involves release of hydrogen at the interface may therefore be incorrect [4]. However, there has been a report that SILC (under F–N stress) is suppressed by deuterium pyrogenic oxidation [7]. This was found that the deuterium incorporation in the entire SiO_2 film suppressed the deterioration of gate oxide due to F–N stress. Although it is known that treatment with deuterium instead of hydrogen in CMOS fabrication provides a possible solution for the reliability, the

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isotope effect on the generation of oxide trap has not yet been fully clarified.

In this work, we present investigations of the deuterium effect on gate oxide degradation under direct tunneling stress condition at elevated bias temperature. We anneal the devices under high-pressure (5 atm) conditions to introduce higher deuterium concentrations into the oxide than is introduced under atmospheric conditions. Through the stress experiments with a constant voltage below impact ionization scale, we find a relatively small but clear suppression of devices-parameter variations and of the gate leakage current. Our results prove that gate oxide degradation is related to the density of hydrogen-related bonds that could act as latent defect or precursor for the oxide trap.

2. Experimental

Both p- and n-MOSFET's were fabricated using standard CMOS processes for various channel lengths and widths down to 0.15 μm. The oxide thickness was 3 nm electrically. The gate oxide films were produced with a conventional furnace in H_2–O_2 ambient. The forming gas annealing was performed at the back end of the process line. Transistors from a given wafer were divided into two groups. One group was annealed in H_2 and the other group was annealed in D_2, both at 450 °C for 3 h and at a pressure of 5 atm. A gate voltage of $V_g = -2.5$ to -4.0 V was applied to the MOSFET gate at the temperature of 100 °C to accelerate gate oxide degradation when the source and drain terminals are connected to the substrate and grounded. For gate oxide leakage current measurements, large area MOSFET's ($W/L = 32/32$) were used to avoid the edge effect. Shifts of threshold voltage (ΔV_{TH}) and the percent shifts (%) of saturation drain current (I_d) were measured to determine device parameter degradation. The threshold voltage was determined under saturation conditions as the gate bias at which $I_d = 40\ \text{nA} \times W/L$. The percent shifts (%) of the gate current (I_g) were also monitored to assess gate oxide reliability.

3. Results

The carrier separation experiments were conducted to measure the gate current I_g, the sum of source and drain currents I_{ds}, and the substrate current I_{sub} separately before stress, applying negative polarity of V_g. All currents flowing into the device are taken as positive.

Fig. 1 shows I_g, I_{sub}, and I_{ds} versus sweeping V_g in our p- (a) and n-MOSFET (b) at 100 °C, respectively. In p-MOSFET, the conduction mechanism for three current components indicates that the electron current, when tunneled to the substrate, produces electron–hole pairs by impact ionization from near $V_g = -4.0$ V. The impacted ionized holes flow out through the source/drain; hence, those "hot" holes generate negative I_{ds}. Below $V_g = -4.0$ V, "cold" hole injection from silicon valence band and electron injection from polysilicon valence band become allowed, simultaneously. In n-MOSFET, the trend is quite similar to the case of p-MOSFET. However, I_{ds} measured the electron current and I_{sub} measured the hole current. Near $V_g = -3.5$ V, the increase of I_{sub} tends to slow down, and changes the sign from positive to negative that means the impact ionization could be dominant [8].

We now focus on the generation of oxide traps that depends on stress voltage levels. Fig. 2 shows the shift of V_{TH} of p- and n-MOSFET's that were stressed using negative bias under the temperature of 100 °C. Bias voltage were chosen to be $V_g = -2.8$, -3.4, and -4.0 V. The commonly observed increase of V_{TH} in p-MOSFET's, which is attributed to the creation of positively charged centers, is suppressed by the deuterium annealing. However, the shifts of V_{TH} in n-MOSFET's are qualitatively different from those in p-MOSFET's. For low bias voltage (region 1), the devices show a decrease of V_{TH} that can be attributed to the creation of positively charged defects. However, for higher bias voltage (region 2), V_{TH} increases, which points toward trapped negative charges. Therefore, deuterium annealing suppresses both positive and negative charge generation in gate oxide of n-MOSFET's.

The shift of threshold voltage is caused by defect generation at both interface and bulk of gate oxide film. The

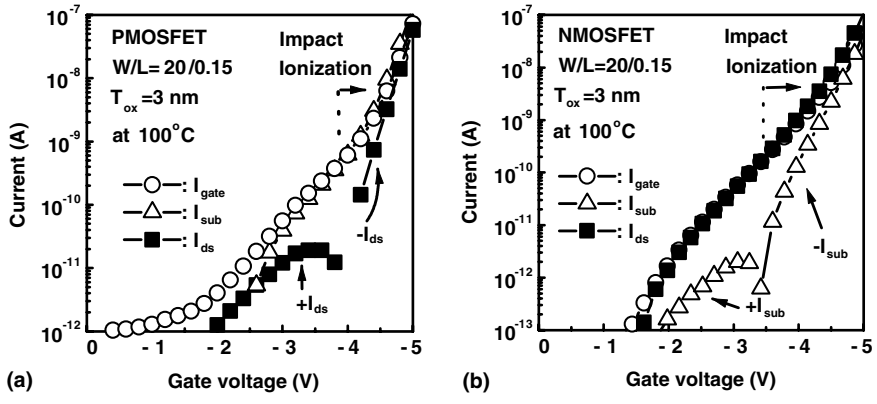

Fig. 1. Carrier separation I–V curves for 3 nm-thick gate oxide devices (W/L: 20 μm/0.15 μm) measured in negative bias: (a) p-MOSFET; (b) n-MOSFET.