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Characterization and strain gradient optimization of PECVD poly-SiGe layers for MEMS applications

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Abstract

Poly-SiGe offers an attractive alternative for low temperature MEMS post-processing above CMOS. This paper presents several investigations made to obtain a crystalline material with excellent mechanical (low stress, low stress gradient) and electrical (low resistivity) properties. Two different techniques were used to enhance the crystallization of the plasma enhanced chemical vapor deposition (PECVD) layers at low temperatures. The use of a high hydrogen dilution ($H_2/(SiH_4 + GeH_4) \approx 90$) leads to microcrystalline SiGe (μcSiGe:H) at temperatures as low as 350 °C. In this work ∼0.6 and 2 μm thick μcSiGe:H layers were characterized and optimized. Alternatively, a chemical vapor deposition (CVD) crystallization layer can be used below the PECVD layer in order to deposit thick (4–10 μm) polycrystalline films of high quality at temperatures around 450 °C. For both layers, the strain gradient can be optimized by the use of a compressive top layer. In the case of the μcSiGe:H layers an alternative new strain gradient optimization method, which uses a variable hydrogen dilution to effectively fine-tune the mechanical properties of the μcSiGe films, is presented. Also new results on the surface roughness of the layers are presented.
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1. Introduction

Polycrystalline-SiGe (poly-SiGe) has been demonstrated to be an ideal material for post-processing MEMS above CMOS, since films with very good electrical and mechanical properties can be obtained at CMOS-compatible temperatures [1,2]. Alloying Si with Ge lowers the melting point and the amorphous to crystalline transition temperature, and therefore also the thermal budget needed to obtain good MEMS structural layers is lowered. Using methods such as multi-layer deposition [3], a high hydrogen dilution [3,4], laser annealing and metal-induced crystallization [5] can lower the deposition temperature further (350–450 °C). The first part of this work deals with the development of microcrystalline SiGe as a high quality material for MEMS applications. The theoretical background of the hydrogenated microcrystalline SiGe (μcSiGe:H) deposition process was discussed in detail in [4]. A study of films of ∼0.6 and 2 μm thickness is presented. To optimize the strain gradient a compressive top layer can be used. Also a new method for strain gradient fine-tuning is introduced: by varying the hydrogen dilution ratio ($H_2/(SiH_4 + GeH_4)$) during layer deposition it is possible to influence the structure of the SiGe crystals, resulting in a different stress profile in the film. Also with this method the strain gradient can be minimized. Furthermore, a multi-layer stack combining chemical vapor deposition (CVD) and plasma enhanced chemical vapor deposition (PECVD) depositions at 450 °C is presented, resulting in films with excellent electrical and mechanical properties grown at a high deposition rate. This process is very useful for applications where thick (4–10 μm) MEMS structural layers with very low strain gradients need to be deposited above standard CMOS [6]. The strain gradient of these multi-layer films was also optimized by the use of a compressive top layer.

2. Experimental

2.1. Deposition

Crystalline SiGe layers were deposited in an Oxford plasma technology (OPT) Plasma lab 100 cold-wall PECVD system,

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which uses a standard parallel plate reactor. A gas flow of 10% germane (GeH_4) in hydrogen (H_2) was used as germanium (Ge) source. The silicon source was a flow of pure silane (SiH_4). The ratio of the silane to germane (SiH_4/GeH_4) flows determines the Ge concentration in the film. Doping of the layers is done using a 1% diborane (B_2H_6) in H_2 as boron (B) gas source (p-type SiGe). The exact doping level will influence the stress in the layers [7], but this was not investigated within this work. The layers are deposited on 6- or 8-in. silicon wafers (1 0 0) having a SiO_2 layer on top.

Rutherford back scattering (RBS) was used to determine the Si and Ge concentration in the layers. A four-point probe was used for the sheet resistance measurements. Morphology and grain microstructure were investigated with transmission electron microscopy (TEM).

The average stress was determined by measuring the curvature of the wafer, before and after deposition of the layers, using an Eichhorn & Hausmann MX 203 stress-meter. The poly-SiGe layers were patterned and plasma etched in a deep dry etching system from surface technology systems (STS) using an $SF_6 + O_2/C_4F_8$ alternating plasma. The thickness of the layers was measured with a stylus profilometer (DekTak). Cantilevers were released after that by removing the underlying sacrificial thermal SiO_2 using HF (49%) vapor at 35 °C. The cantilever profile and tip deflection were measured using a Wyko profilometer from VEECO. The deflection data is used to calculate the strain gradient in the film.

2.1.1. Microcrystalline deposition process

μcSiGe layers are deposited at 1 Torr pressure. The plasma power used is 370 mW/cm^2. Experiments were performed at 350 and 400 °C deposition temperatures. For the single films and the films with compressive top layer, a hydrogen dilution ($H_2/(SiH_4 + GeH_4)$) of approximately 90 was used. The H_2 and B_2H_6 flows were kept constant throughout the deposition at 2 slm and 10 sccm, respectively, while the SiH_4/GeH_4 was variable, determining the Ge content in the grown film.

For the variable hydrogen dilution depositions (see Section 3.1.2.2) $H_2/(SiH_4 + GeH_4)$ ratios as high as 90 (2 slm H_2 flow) were used at the start of the deposition, followed by steps with a gradually decreasing hydrogen flow.

2.1.2. Multi-layer combining CVD and PECVD

The multi-layers are deposited at 2 Torr pressure, 450 °C and 0 W power (no plasma) for the (LP)CVD part of the layer. The PECVD parts of the layer are normally deposited at 30 W (power density 61 mW/cm^2) except for the compressive top layer deposited at high plasma power (40 W). No extra hydrogen dilution was used for these films. A constant B_2H_6 flow equal to 40 sccm was used during the deposition of the entire layer. A SiH_4/GeH_4 ratio of 2.4 was used for the whole layer stack except for the Si-rich top compensation layer and the a-Si seed layer.

3. Results and discussion

3.1. Microcrystalline deposition process

3.1.1. Single film characterization

Fig. 1 shows the TEM cross-sections of as-grown thin (∼0.6 μm thick) single microcrystalline SiGe layers deposited at 350 °C with different Ge content. The pure Ge layer is completely amorphous (Fig. 1a), while the pure Si layer is fully crystalline (Fig. 1b) and consists of fine grains. SiGe layers have well defined almost columnar grains and a small amorphous fraction at the SiO_2/SiGe interface (Fig. 1c). The surface roughness of these layers was measured using an atomic force microscope (AFM), and the root-mean-square (RMS) values are presented in Fig. 2. The surface roughness gradually increases with increasing Ge content in the layer. For example, the RMS value is 4.6 nm for a film with 44% Ge, while the RMS value is 7.3 nm in the case of a film with 69% Ge. It is worth noticing the two extreme cases: a pure Si layer has a roughness of 5.7 nm, while the pure Ge layer has a roughness of only 4 nm. This is to be expected since the pure Ge layer is completely amorphous, as proven by the TEM image (Fig. 1a). This means that the use of the high hydrogen dilution is much more efficient in obtaining crystalline layers at low deposition temperatures in the case of SiGe and Si than in the case of pure Ge, as also

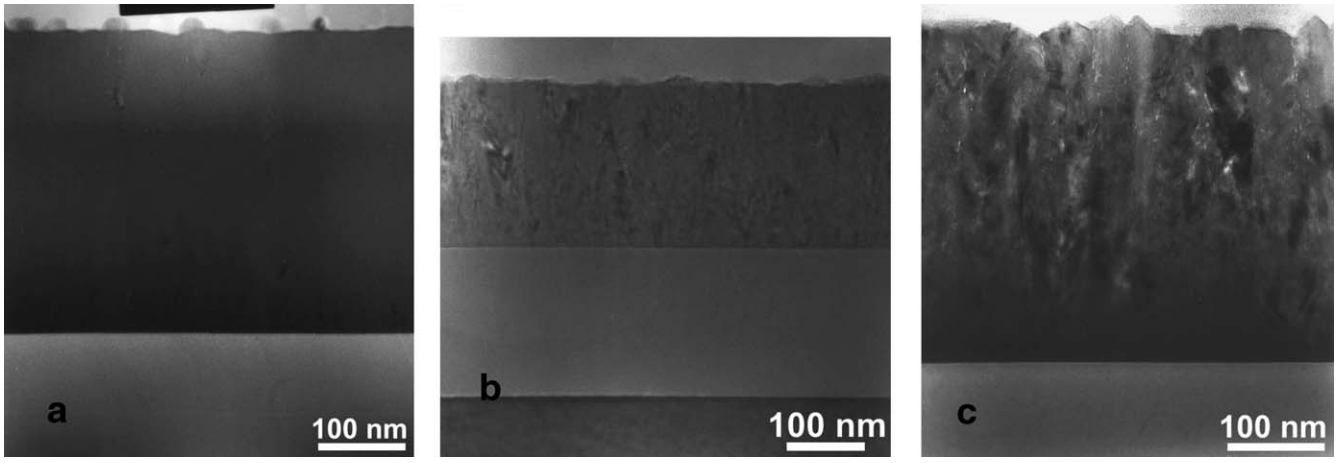

Fig. 1. Cross-section TEM of as-deposited single layers deposited at 350 °C—(a) pure Ge: completely amorphous; (b) pure Si: fully crystalline, consisting of fine grains; (c) μc$Si_{34}Ge_{66}$: well defined columnar grains, small amorphous fraction at the SiO_2/SiGe interface.

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