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Letter

Modeling the zero and forward bias operation of PIN diodes for high-frequency applications

N.V. Drozdovski, L.M. Drozdovskaia, R.H. Caverly *, M.J. Quinn

Villanova University, 800 Lancaster Avenue, Villanova, PA 19085, USA

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Abstract

Silicon-based PIN diodes have been studied in a high-frequency switching application under moderate to high input voltage levels. A model suitable for full circuit simulators such as SPICE is proposed and tested. The model accurately describes the impedance behavior over changes in frequency, DC bias current and applied voltage level. A localized maximum in series resistance is accurately modeled and found to be a function of the diode's transit time effect. The model also describes the nonlinear high current stored charge-DC bias current effect. The full circuit PIN diode model is verified with experimental observations.

Keywords: PIN diode; Computer modeling; Control applications

1. Introduction

The PIN diode is widely used in many RF and microwave systems, including wireless mobile communications systems [1]. Switching and signal level control (attenuation) of signals in these systems are provided mainly by silicon (Si) PIN diodes, with their gallium arsenide (GaAs) counterparts used in some specialized control systems. The main linear circuit parameters that microwave and RF engineers use when designing systems including these control devices are insertion loss and isolation for switch applications and attenuation level for attenuators. A number of publications have been written describing various control design techniques that use these devices in a variety of applications for example, [2–4]. Although PIN diodes have been used in microwave and RF control systems for more than 40 years, many aspects of the diode's behavior are still not well understood. Some of these less understood modes of operation include the PIN diode's nonlinear behavior under forward bias and zero bias operation. In these cases, the so-called linear operation of the device, based on linear design techniques, can be adversely affected by these nonideal properties. For example, the PIN diode impedance has traditionally been assumed to be independent of the applied power level. However, measurements show that the impedance increases as incident power increases, which can manifest itself in power-dependent insertion loss or attenuation in circuits using these devices [5].

The key to understanding PIN diode behavior rests with understanding the role of the injected carrier density in the I-region of the device and the interaction of these carriers with the boundary regions. Various approaches have been used to model the carrier density in the I-region as a function of applied forward bias. These models can be classified in the broad categories of numerical [6,7], analytical [8] and full circuit simulation [2,4,9]. Numerical models are useful because they offer a detailed study of the device under a wide variety of operating conditions. Their extensive computation load, however, limits their usefulness for full circuit simulation. Analytic models are useful because they provide

* Corresponding author: Tel.: +1-610-519-5660; fax: +1-610-519-4436.

E-mail address: caverly@ece.vill.edu (R.H. Caverly).

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closed form solutions that yield rapid computation times, but these models are limited in usefulness for full circuit simulation since they are often derived under a restrictive set of operating conditions. Full circuit simulation of a solid-state device requires a modeling structure that provides rapid, accurate calculation under a variety of operating conditions. The work described in this paper is an investigation into the development of a model suitable for use in full circuit simulators such as SPICE. This model is compared with simulation results using a simple analytic model [8] and an isothermal one-dimensional drift–diffusion model [7] based on numerical techniques. Another aim of this paper is to illustrate the full circuit simulation model for the PIN diode under several circuit operating conditions. The model presented is suitable for circuit simulators such as SPICE and APLAC and includes provisions for computation of the self-rectified PIN diode current in self-biased applications. The model results are compared with experimental data showing the validity of the full circuit simulation model.

2. Theory and analysis

The typical PIN diode is fabricated as a mesa structure with a heavily doped substrate, a high-resistivity epitaxial layer grown on this substrate, and a heavily doped cap. The PIN diode is composed of P^+ and N^+ heavily doped semiconductor layers separated by a lightly doped P-type (or N-type) layer generally referred I-region. With this structure, three regions need to be considered for any modeling effort to succeed with matching boundary conditions: the P^+–I-layer boundary, the I-region itself, and the N^+–I-layer boundary. The two heavily doped boundary regions are the sources of injected I-region holes and electrons, which increases the I-region conductivity under forward DC bias. At zero or small forward bias, the electron–hole injection level is low but can have a significant impact on the impedance component due to the background resistivity and natural geometric capacitance. The I-region carrier concentration under all bias levels is modeled using the ambipolar carrier transport equation:

$$\frac{\partial^2 n(x,t)-n_0}{\partial x^2}=\frac{n(x,t)-n_0}{D_a\tau}+\frac{1}{D_a}\frac{\partial n(x,t)-n_0}{\partial t} \tag{1}$$

where n_0 is the constant I-region background carrier concentration, the carrier lifetime τ is a function of total I-region carrier concentration $n(x,t)$, and D_a is the ambipolar diffusivity. Under high injection, the term n_0 is much less than $n(x,t)$ and is usually neglected. The term n_0 begins to dominate as the bias approaches zero and cannot be neglected under these operating conditions. It is the total charge in the I-region that governs such PIN diode behavior as the impedance frequency characteristic, insertion loss and limiter action. This stored charge phenomenon and its relationship to current injection from both the P–I and I–N junctions must be accurately modeled regardless of the simulation technique used (full circuit, numerical or analytical).

For full circuit simulation modeling, the P^+–I and I–N^+ boundary regions may be characterized by the default simulator PN junction diode circuit elements. Modeling the I-region is more problematic in the full circuit simulator case since this region exhibits charge storage phenomenon, which is manifested in the charge–current (or Q–I) relationship. This phenomenon can be described by default circuit simulator elements. For the full circuit model, Eq. (1) must couple with models of the P–I and I–N junctions. From Eq. (1), a relationship between the stored charge in the I-region and the current flowing through the diode can be written as:

$$I(s)=Q(s)\frac{L_a\sqrt{1+s\tau}}{x_m\tau}\tanh\left(\frac{x_m}{L_a}\sqrt{1+s\tau}\right)+I_o \tag{2}$$

where I_o is the external DC bias current, L_a is the ambipolar recombination length ($\sqrt{D_a\tau}$), and x_m (the minimum of the I-region stored charge density) is given by:

$$x_m=\frac{W}{2}\left[1+\frac{2\lambda}{W}\tanh^{-1}\left(\frac{b-1}{b+1}\tanh\left(\frac{W}{2\lambda}\right)\right)\right] \tag{3}$$

b is the electron to hole mobility ratio, W is the I-region thickness, $\lambda=L_a/\sqrt{1+s\tau}$, $s=j\omega\tau$, and the other symbols have their usual meanings. The term x_m reduces to $W/2$ for equal hole and electron nobilities, an assumption that has been shown to have negligible effects on simulations [10]. Eq. (2) can be transformed to a form usable in full circuit simulators by noting that if the stored charge $Q(s)$ excites a circuit, then the response will be the current $I(s)$. A transfer function $H(s)$ relating the current through the diode with the charge stored in the I-region can be defined as $H(s)=Q(s)/I(s)$. As a transfer function, circuit synthesis approximations and techniques are used to derive an equivalent circuit representation that allows circuit simulators to solve for the temporal and overall frequency response in the stored charge region. A passive ladder network describing the Q–I relationship can be synthesized using all resistive and capacitive elements by a Pade approximation for the general equation form $x\tanh(x)$ [10]:

$$H(s)=\cfrac{1}{Z+\cfrac{1}{\cfrac{3}{T}+\cfrac{1}{5Z+\cfrac{1}{\cfrac{7}{T}+\cdots}}}} \tag{4}$$

where $Z=\tau/\sqrt{1+s\tau}$ and $T=x_m^2/D_a$. An RC ladder network that approximates the Q–I relationship for the