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Letter

A novel approach to quantitative determination of charge trapping near channel/drain edge in MOSFETs

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Abstract

In this letter, we report a novel approach to quantitative determination of charge trapping near the channel/drain edge caused by electrical stress. The approach is based on gate-controlled-diode (GCD) measurement. By measuring the GCD drain current in the band-to-band tunneling regime and using the formula developed in this work, the change of the Si surface field resulting from the charge trapping can be calculated instantly, and then the charge trapping is determined quantitatively. It is found that the stress-time dependence of both the surface field change and the charge trapping follow a power law.

Keywords: Device characterization; Gate-controlled-diode measurement; Charge trapping; MOS devices

1. Introduction

It is well known that when the gate oxide is subjected to electrical stress such as Fowler–Nordheim (FN) or hot-carrier injections there is trap generation as well as charge trapping both at the interface and in the gate oxide. Enhanced electron trapping near channel edge in MOSFETs after FN or channel hot-electron injection has been observed [1,2]. The edge trapping effect could increase the electrical channel length or channel resistance [1]. It was also reported that the charge trapping could also enhance the hot-carrier stress-induced drain leakage current degradation [3]. For deep submicron devices, the trapping near the channel edges could be a concern. Therefore, a reliable characterization technique capable of quantitative determination of the charge trapping is required. In this letter, we briefly report a new approach that is based on the gate-controlled-diode (GCD) measurement [4,5]. By measuring the GCD drain current in the band-to-band tunneling regime and using the formula developed in this work, the change of the Si surface field resulting from the charge trapping near the channel edge can be calculated instantly, and then the charge trapping is determined quantitatively. It is found that the stress-time dependence of the charge trapping follows a power law.

2. Experiment

The devices used in this study were polysilicon-gate n-channel MOSFETs with a channel length of 0.25 μm and a gate width of 50 μm. The gate oxide thickness was 4 nm. The devices were stressed with FN injection under a constant current with a current density of 5.3 mA/cm^2. The GCD measurements were carried out before and after each FN stress. Fig. 1a shows the bias configuration (source floating) of the MOSFET under test for the GCD measurements. In the GCD measurement, the gate voltage was swept from a sufficiently negative voltage (which corresponds to the band-to-band tunneling

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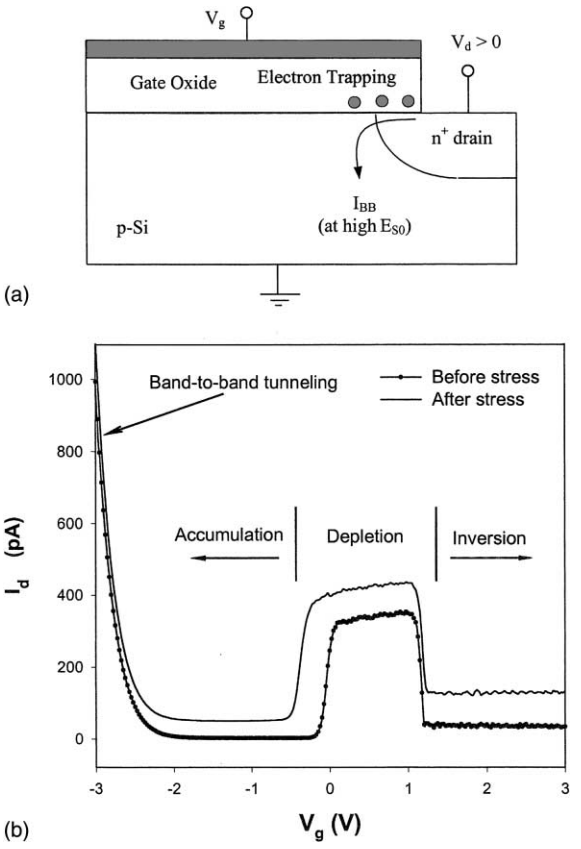

Fig. 1. (a) Bias configuration (with source floating) for the GCD measurement and the illustration of charge trapping near the channel/drain edge. (b) Typical GCD characteristics of an n-channel MOSFET before and after FN stress.

under strong accumulation) to a sufficiently positive voltage (which corresponds to strong inversion), while the drain was kept at a constant positive voltage (+1 V) and the substrate was kept at 0 V. Both the FN stress and the GCD measurements were carried out with a HP4156A semiconductor parameter analyzer at room temperature. Fig. 1b shows the examples of the GCD characteristics before and after stress. As can be seen in this figure, the stress caused very significant changes in the situations including the accumulation (before the band-to-band tunneling), depletion and inversion. The changes are attributed to the interface trap generation, and the details will be published elsewhere. In this study, we are concerned with only the band-to-band tunneling current in the strong accumulation regime, because we can determine the charge trapping near the channel edge by measuring this current. For the measurement of the band-to-band tunneling current, the gate current was monitored also to make sure that the contribution of the gate oxide leakage was insignificant.

3. Method and results

As shown in Fig. 1, at sufficiently high Si surface electric field E_s under strong accumulation, the reverse drain current is dominated by the band-to-band tunneling current. The band-to-band tunneling current is given by [3]

$$J = AE_s^2 \exp(-B/E_s) \tag{1}$$

where A and B are two constants. When the device is subjected to an electrical stress, there are charges trapped in the gate oxide near the channel/drain edge (as shown in Fig. 1a), and this leads to a change in the Si surface field. The Si surface field can be written as

$$E_s = E_{s0} + \Delta E = E_{s0}(1 + \Delta E/E_{s0}) \tag{2}$$

where ΔE is the change in the Si surface field due to the charge trapping caused by the stress. ΔE is given by

$$\Delta E = Q_{ox}/\varepsilon_{Si} \tag{3}$$

where ε_{Si} is the Si dielectric constant, and Q_{ox} is the charge trapping defined as the equivalent areal density at the Si/SiO_2 surface. The Si surface field E_{s0} before stress, which is equal to the applied Si surface field, can be determined in the way described in [6]. If the charge trapping is taken into account

$$J = AE_{s0}^2(1 + \Delta E/E_{s0})^2 \exp\left[-\frac{B}{E_{s0}}\frac{1}{(1 + \Delta E/E_{s0})}\right] \tag{4}$$

Eq. (4) indicates that the charge trapping will cause a change in the band-to-band tunneling current. This is confirmed by the experimental results shown in Fig. 2, in

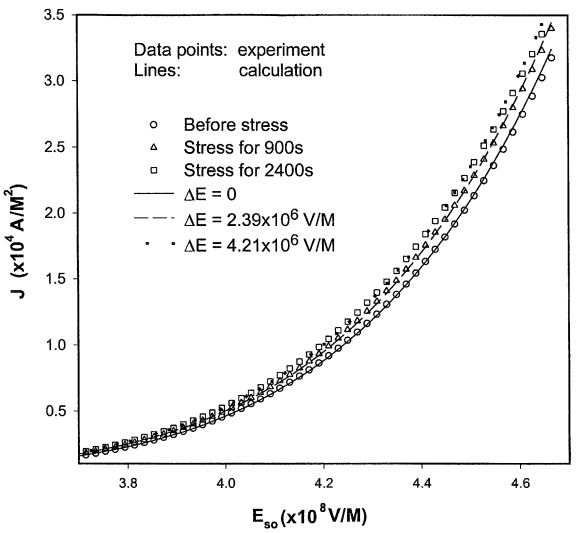

Fig. 2. Comparison between the measurement and the calculation for the band-to-band tunneling current under strong accumulation.