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Letter

Instability investigation of $In_{0.7}Ga_{0.3}As$ quantum-well MOSFETs with Al_2O_3 and Al_2O_3/HfO_2

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ABSTRACT

We present an instability investigation of $In_{0.7}Ga_{0.3}As$ quantum-well (QW) metal–oxide–semiconductor field-effect-transistors (MOSFETs) on InP substrate with Al_2O_3 and Al_2O_3/HfO_2 gate stacks. The device with bi-layer Al_2O_3/HfO_2 gate stack exhibits larger shift in threshold-voltage (ΔV_T) under a constant-voltage-stress condition (CVS), than one with single Al_2O_3 gate stack. At cryogenic temperature, the device with bi-layer Al_2O_3/HfO_2 gate stack also induces worse hysteresis behavior than one with single Al_2O_3 gate stack. These are mainly attributed to more traps inside the HfO_2 material, yielding a charge build-up inside the HfO_2 gate dielectric. This strongly calls for a follow-up process to minimize those traps within the high-*k* dielectric layer and eventually to improve the reliability of InGaAs MOSFETs with HfO_2-based high-*k* gate dielectric.

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1. Introduction

Indium-rich $In_xGa_{1-x}As$ channel materials, $x > 0.53$, have re-gained their interest, and now stand out as the most promising non-Si *n*-channel material for next-generation low-power and high-performance logic applications at 5-nm technology-node and/or beyond [1–3]. This is a consequence of their superior electron carrier transport properties, such as electron mobility ($\mu_{n,Hall}$) in excess of 10,000 cm^2/V-sec and electron injection velocity (v_{inj}) over 3×10^7 cm/s at room temperature [4,5]. To maximize benefits of using III–V channel materials with high electron mobility, it is of critical importance to minimize all the traps, associated with high-*k* dielectric layers adjacent to III–V channel materials. In fact, those traps deteriorate a subthreshold-swing (*S*) and mobility in the channel and therefore degrade an I_{ON}/I_{OFF} ratio[4]. To date, there are only a few reports on relevant reliability issues in InGaAs MOSFETs [6,7]. A charge-trapping mechanism in the high-*k* dielectric materials during device operation can cause a frequency dispersion and shift in V_T (ΔV_T), causing a severe reliability concern [6,7].

In our previous works, we reported on $In_{0.7}Ga_{0.3}As$ quantum-well (QW) MOSFETs with equivalent-oxide-thickness (EOT) of less than 1 nm, using a bi-layer Al_2O_3/HfO_2 gate stack [8]. In this paper, we carry out a comprehensive reliability study on InGaAs MOSFETs with single-layer Al_2O_3 and bi-layer Al_2O_3/HfO_2 III–V gate stacks, in an effort to identify the impact of traps in different high-*k* dielectric layers. In addition, we perform a cryogenic DC measurement for $In_{0.7}Ga_{0.3}As$ QW MOSFETs to try to freeze out traps at the interface (D_{it}) between $In_{0.7}Ga_{0.3}As$ channel and high-*k* dielectric layer. Clearly, we observe that the device with bi-layer Al_2O_3/HfO_2 gate stack induces more charge-trapping phenomena than one with Al_2O_3 gate stack.

2. Process technology

Fig. 1(a) and (b) shows a cross-sectional cartoon of an $In_{0.7}Ga_{0.3}As$ quantum-well (QW) MOSFET with high-*k* gate stacks

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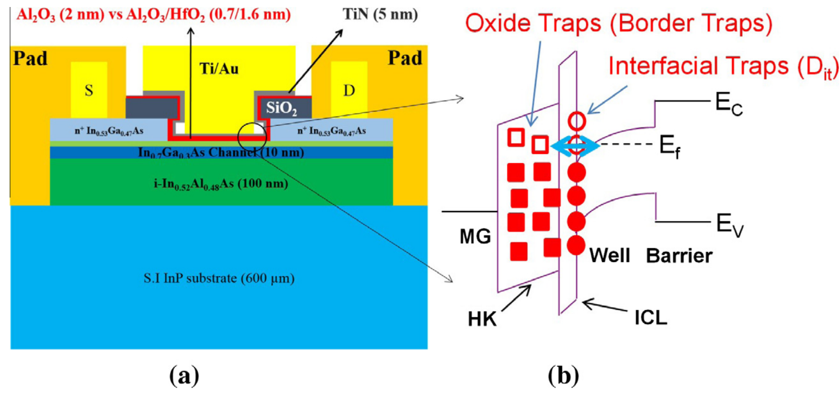

Fig. 1. (a) Cross-sectional cartoon of an $In_{0.7}Ga_{0.3}As$ quantum-well (QW) MOSFET, and (b) energy-band diagram of III–V gate stack with bi-layer dielectric scheme, highlighting the interaction of channel carriers with interface traps and oxide traps (in other words, border traps).

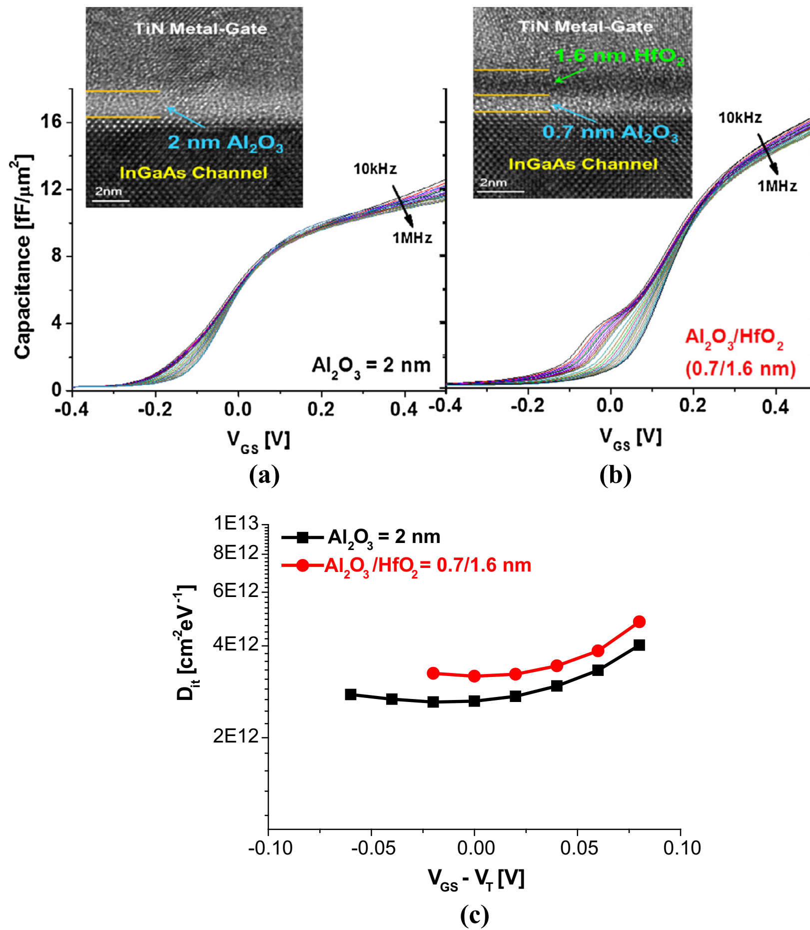

Fig. 2. C–V_{GS} measurement at V_{DS} = 0 V for planar QW MOSFETs with Al_2O_3 (a) and Al_2O_3/HfO_2 (b), and D_{it} extraction using conductance method (c). Inset is High-resolution TEM images for single-layer Al_2O_3 (a) and bi-layer Al_2O_3/HfO_2 (b) on top of InGaAs. Both C–V_{GS} curves shows small frequency dispersion in strong accumulation region, and the hump near off-state is a consequence of D_{it}. For device with Al_2O_3/HfO_2 gate stack, the measured C_g is 16 fF/μm^2 at (V_{GS}–V_T = 0.5 V), the highest in any QW-MOSFETs.

and an energy-band diagram for InGaAs gate stack with bi-layer dielectric scheme, highlighting the interaction of channel carriers with interface traps and oxide traps, so called "border traps". After high-*k* gate stack deposition to an $In_{0.7}Ga_{0.3}As$ channel, a TiN metal-gate (MG) with 5 nm was deposited in an *in-situ* manner by ALD. Generally, the interface control layer (ICL) requires a defect-free interfacial oxide with large energy-band offset, and the 2nd dielectric layer offers higher dielectric constant (k) to enable an aggressive equivalent–oxide–thickness (EOT) scaling while mitigating an increase in the gate leakage current. After a formation of dummy-gate (DG) using Hydrogen–Silses–Quioxane (HSQ) resist, a heavily doped $In_{0.53}Ga_{0.47}As$ is grown selectively on source and drain region by MOCVD. Here, Si is used as an n-type dopant and a growth temperature of the reactor is 600 °C. Metal–Organic (MO) sources and reactant gas are Tri-Methyl Indium (TMIn), Tri-Methyl Gallium (TMGa), and arshine (AsH_3) gases with V/III ratio of 94. Doping concentration of the optimized $In_{0.53}Ga_{0.47}As$ contacts is as high as $3 \times 10^{19}/cm^3$. Then, mesa

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