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A 72% error reduction scheme based on temperature acceleration for long-term data storage applications: Cold flash and millennium memories

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ABSTRACT

A solid-state drive (SSD) with 1Xnm triple-level cell (TLC) NAND flash is proposed for low cost data storage applications with long-term data-retention requirements. Specifically, cold data storage requires 20 years data-retention with 100 write/erase (W/E) cycles, whereas digital archive storage requires 1000 years retention time with 1 W/E cycle. To achieve these requirements, a flexible-*n*LC scheme is proposed to improve the reliability of 1Xnm TLC NAND flash (Yamazaki et al., 2015). The proposed scheme combines two schemes, *n*-out-of-8 level cell (*n*LC) (Tanakamaru et al., 2014) and asymmetric coding (AC) (Tanakamaru et al., 2012) with the addition of a vertical flag. By measuring 1Xnm TLC NAND flash memory, the proposed scheme reduces errors by 72% and 69% for digital archive and cold flash respectively, compared to the conventional *n*LC scheme.

1. Introduction

The solid-state drive (SSD) has the advantages of fast write and read speeds and high reliability compared with other types of data storage such as the hard disk drive and optical disk drive. SSDs are also highly reliable because, unlike hard disk and optical drives, they do not include mechanical components, which might malfunction due to physical wear and tear. Therefore, SSDs are well-suited to store cold data and archive data on enterprise servers, which need 20 and 1000 years retention time, respectively [1]. In this work, 1Xnm TLC NAND flash is used to achieve the lowest cost storage system, due to its capacity to store 3 bits in one memory cell [4]. However, the reliability of 1Xnm TLC NAND flash is lower compared with previous NAND flash generations that have larger cell size, or store fewer bits per cell [5]. In the small cell size of the 1Xnm generation, the number of electrons stored in the floating gate is significantly lower, which negatively impacts data-retention time [6]. In addition, because there are 8 possible threshold voltage (V_{TH}) levels in the TLC NAND flash cell, the voltage margins between V_{TH} levels are narrower than in the multi-level cell (MLC) and single-level cell (SLC) NAND flash, which have 4 and 2 V_{TH} levels, respectively. The reduced V_{TH} margins in 1Xnm NAND flash causes higher bit-error rates (BERs), which requires higher error correction ability to recover the errors, and also effectively degrades the data-retention time. Thus, the reliability of the 1Xnm TLC NAND flash SSD needs to be improved to simultaneously realize low cost and long-term data storage for 20–1000 years.

In NAND flash memory, reliability errors are mainly caused by program-disturb (PD), read-disturb (RD) and data-retention (DR), as described in Fig. 1. PD error and RD error are caused by an increase in V_{TH} due to the unwanted electron injection into the floating gate (FG) during program and read respectively [7]. On the other hand, DR error is caused by electron ejection from the FG and leads to decrease in V_{TH} [8].

During program, 2 types of voltage conditions can induce electron injection. First, in pass-through voltage (V_{pass}) disturb, all the unselected cells in the selected bit line experience a gate–source voltage of around 10 V. The second V_{pgm} type of disturb occurs in the inhibited cells in the selected word line (WL) due to the potential difference between V_{pgm} (18 V) and program inhibit BL voltage (8 V).

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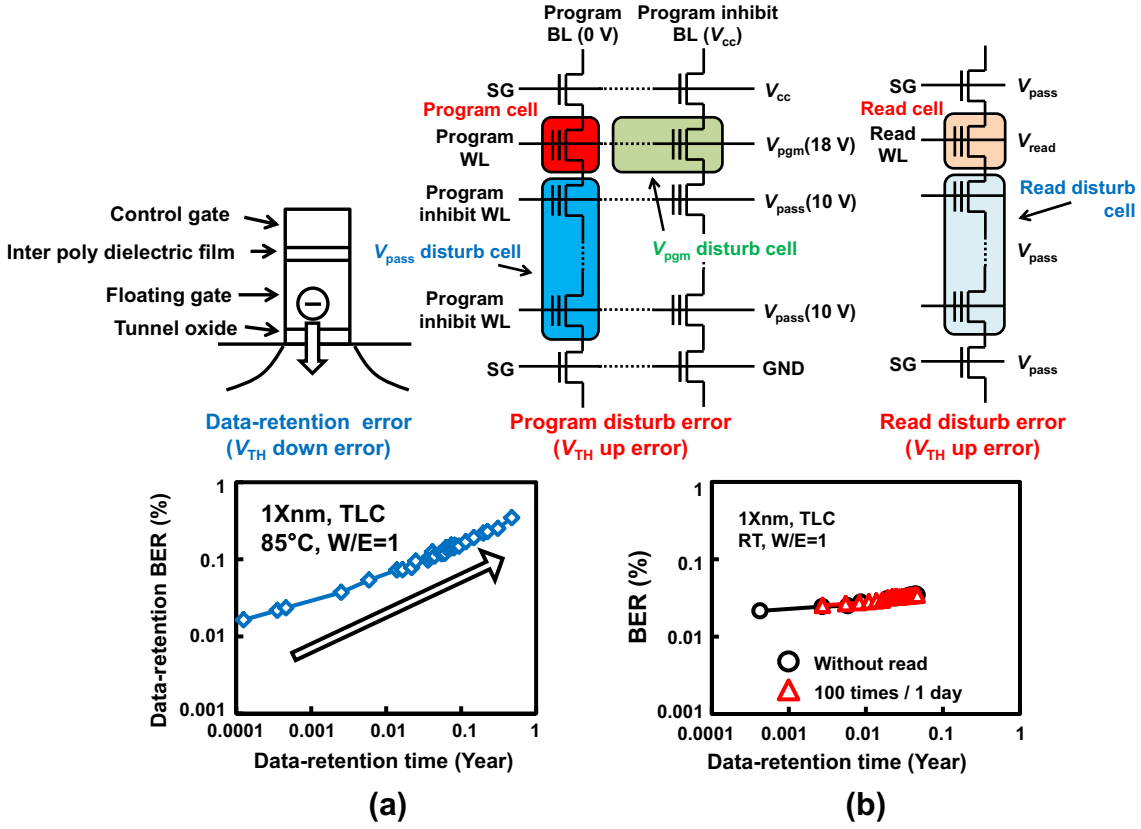

Fig. 1. (a) Measured DR error in 1Xnm NAND flash memory and (b) influence of read operation in long-term storage.

Similarly, when NAND cells are read, read V_{pass} is applied to all the unselected WL's in the NAND block. Compared to PD, RD is a weaker effect because the read V_{pass} voltage is lower.

Fig. 1(a) shows measured bit-error rates (BERs) from a 1Xnm TLC NAND flash memory array. Bit error rate is calculated based on errors that occur in a single NAND block, which is 2 MBytes. As data-retention time increases, DR errors also increase and can become more than 100 times higher than PD errors [3]. In long-term storage, the data is not frequently read [9]. Even when read frequency is 100 times per a day, there is little difference in BER compared with BER without read disturb. Therefore, in long-term storage, RD error is negligibly small. Thus, reducing the DR errors is key to improve NAND flash reliability and obtain long-term data-retention.

Conventionally, schemes *n*-out-of-8 level cell (*n*LC) and asymmetric coding (AC) are applied to 2Xnm TLC NAND flash and MLC NAND flash respectively to reduce DR errors. In scheme *n*LC, "*n*" is the number of cell program levels, which is less than the maximum number of levels, 8. By decreasing the number of possible V_{TH} levels stored on the TLC NAND flash cell, significant BER reduction is obtained. For example, in 2Xnm TLC NAND flash, 10 years data-retention is achieved with 7LC at 85 °C [2]. Note that 7LC achieves the lower cost than TLC (8LC) because TLC requires a stronger by error-correcting code (ECC) and increases the cell area overhead of parity bit [2]. In addition, DR error can be reduced by using the AC scheme, which re-arranges the data to avoid high populations of data in the V_{TH} levels that have high error rates [3].

Fig. 2 shows the required data-retention time and write/erase (W/E) cycles for different applications. Consumer SSD requires moderate endurance, e.g. 3000 W/E cycles and moderate data-retention time, e.g. 3 years. Cold flash is used in social-networking services to store photos and movies, which require infrequent data-programming [10]. Therefore, lower 100-cycles

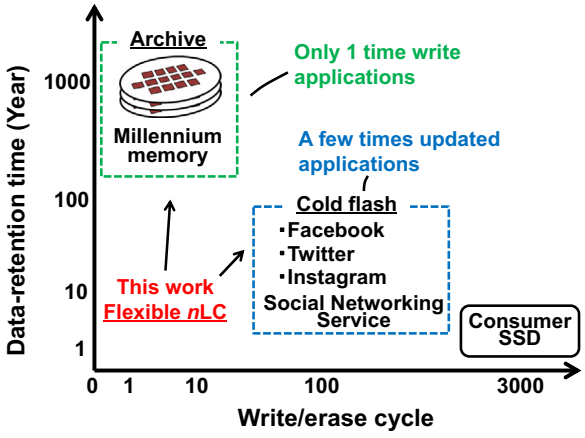

Fig. 2. SSD applications.

endurance and longer 20-year data-retention are needed. Lastly, the digital archive millennium memory requires only one-time write and extremely long >1000 years retention to preserve human digital data such as culture, history and science information [11,12]. Because the 1Xnm TLC NAND flash has higher BERs than 2Xnm TLC NAND flash [13], the conventional *n*LC scheme is not sufficient to meet the requirement of long-term data storage. In this work, the reliability of 1Xnm TLC NAND flash is largely improved with the proposal, called flexible-*n*LC. This scheme combines the conventional schemes *n*LC and AC by proposing an additional vertical flag. Fig. 3 illustrates the architecture of the proposed SSD controller by using the proposed scheme flexible-*n*LC. Our proposed controller adds a "Program data encoder", a "Data flip encoder", a "Data to *n*-base coder" and combines *n*LC