Solid-State Electronics 115 (2016) 7–11

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Investigation of low-frequency noise of 28-nm technology process of high-k/metal gate p-MOSFETs with fluorine incorporation

Tsung-Hsien Kao [a], Shoou-Jinn Chang [a,*], Yean-Kuen Fang [a], Po-Chin Huang [a], Bo-Chin Wang [a], Chung-Yi Wu [b], San-Lein Wu [b]

[a] Institute of Microelectronics and Department of Electrical Engineering, Advanced Optoelectronic Technology Center, Center for Micro/Nano Science and Technology, National Cheng Kung University, Tainan 70101, Taiwan
[b] Department of Electronic Engineering, Cheng Shiu University, Niaosong, Kaohsiung 83347, Taiwan

ARTICLE INFO

Article history:
Received 13 April 2015
Received in revised form 12 August 2015
Accepted 20 September 2015
Available online 24 October 2015

Keywords:
Random telegraph noise (RTN)
High-k/metal gate (HK/MG)
Fluorine incorporation

ABSTRACT

In this study, the properties of dielectric traps by the impact of Fluorine (F) implantation on 1/*f* noise and the random telegraph noise (RTN) of high-k/metal gate (HK/MG) p-type metal–oxide–semiconductor field-effect transistors (pMOSFETs) were investigated. The incorporation of F has been identified as an effective method to passivate oxygen vacancies, defect sites, and reduce the gate leakage current in pMOSFETs. Compared with a control device, the F-implanted HK/MG devices show that the trap positions were closer to the SiO_2 interfacial layer (IL)/Si channel. Furthermore, we found that F implantation could result in a smaller tunneling attenuation length (λ) and smaller slow oxide interface trap density (N_t).

As the complementary metal–oxide–semiconductor (CMOS) device is continuously scaled down into the sub-100-nm regime, the influence of low-frequency noise (LFN) on the circuit performance is more pronounced and being considered due to the 1/*f* noise increases as the reciprocal of the device area. Recent studies indicate that LFN, including 1/*f* noise and random telegraph noise (RTN), is a useful characterization technique for studying slow oxide traps, border traps, or trap activity in the gate dielectric of nanoscale metal–oxide–semiconductor field-effect transistor (MOSFET) devices [1–3]. For high-k/metal-gate (HK/MG) devices, 1/*f* noise exhibits overall oxide trap density for determination of oxide trap effects on the technological process. However, it is inadequate to implement 1/*f* noise for small-area devices (<1 μm^2) owing to the large sample-to-sample variation in noise level. In addition, RTN is attributed to the random trapping/detrapping behaviors of a single trap, resulting in the phenomena of two discrete current levels in the time domains. Through the characterization of RTN, trap parameters can be obtained, including the energy level, capture and emission kinetics, and spatial location [4]. RTN plays a more important role because it can be used to monitor the oxide trap distributions and characteristics that depend largely on the process flow evolution. Therefore, we use the 1/*f* noise and RTN to study oxide traps in small-area devices (<1 μm^2).

In the contrast, high-k (HK) materials and metal gate (MG) electrodes have been widely introduced into CMOS technology to replace SiO_2 dielectrics for the sub-28-nm era and beyond [5,6]. The reliability of this type of dielectric stack is closely linked to the trap distributions that generate RTN. However, fabricating HK/MG p-type MOSFETs (pMOSFETs) with a low threshold voltage (V_T) and a small equivalent oxide thickness (EOT) is still a crucial challenge in gate-first integration, because of the presence of numerous oxygen vacancies and defect sites in the HK gate dielectric [7]. Recently, the incorporation of Fluorine (F) has been identified as an effective method to passivate oxygen vacancies and defect sites, control V_T, and reduce the gate leakage current in pMOSFETs [8–12]. In this letter, we report the fabrication of 28-nm gate-first HK/MG pMOSFETs with F incorporation and with different concentrations. Compared with a control device, we found that the implanted F atoms could effectively passivate the interface charge-trapping sites. With an F implantation dose of 5×10^{15} cm^{-2}, we verified that we can reduce the slow oxide interface trap density (N_t) from 7.94×10^{18} to 1.53×10^{18} cm^{-3} eV^{-1}.

The pMOSFETs used in this study were fabricated using 28-nm gate-first HK/MG technology. The gate dielectrics consist of a ~1-nm-thick thermal-grown SiO_2 interfacial layer (IL), followed by a ~2.5-nm-thick HfO_2 film prepared by atomic layer deposition (ALD). In the F channel implantation experiments, 10 keV implantation was performed with two different F doses (i.e., 2×10^{15} cm^{-2} for device A and 5×10^{15} cm^{-2} for device B) through a ~4-nm-thick sacrificial oxide. After the removal of the

* Corresponding author.
E-mail address: changsj@mail.ncku.edu.tw (S.-J. Chang).

http://dx.doi.org/10.1016/j.sse.2015.09.013
0038-1101/

oxide mask, a fresh core oxide was grown. A rapid thermal processing (RTP) annealing was performed at 930 °C to manipulate the F distribution profile after implantation. A 10-nm-thick TiN layer prepared by radio-frequency physical vapor deposition (PVD) was then deposited on top of the gate dielectrics. On the other hand, it has been shown that aluminum ion implantation (Al I/I) can be employed to achieve a large V_{FB} shift with a minimal EOT penalty in HK/MG pMOSFETs [13,14]. The Al I/I was subsequently performed through TiN following gate metal deposition with implantation energy of 1.2 keV and dose of 5×10^{15} cm^{-2}. A 60-nm-thick poly-gate was then deposited to serve as the low-resistance gate electrode, followed by source/drain (S/D) implantation. RTP spike annealing was then performed again at 1025 °C to activate S/D. Ni silicide was then formed on top of the poly-gate to reduce contact resistance. Finally, 20-min forming gas annealing was performed at 420 °C to passivate the interface states, followed by standard back-end processing steps. For comparison, HK/MG pMOSFETs formed without F were also prepared and labeled as control device. It should be noted that EOT of these devices was all approximately 1.3 nm. The $1/f$ noise measurements were carried out using SR570 low-noise current preamplifiers and Agilent 35670A dynamic signal analyzer. Time-domain RTN measurements were then performed on small-area ($L = 0.04$ μm and $W = 0.25$ μm) pMOSFETs using a waveform generator/fast measurement unit (WGFMU) system based on the Agilent B1500 Semiconductor Parameter Analyzer. To avoid singularity effects and to demonstrate the reproducibility of the oxide trap characteristics, at least six devices were measured to determine the device-to-device variation and ensure that the results are reproducible [1].

Fig. 1 shows the drain current (I_D) as a function of drain voltage (V_D) for the fabricated HK/MG pMOSFETs. It can be seen that I_D was enhanced by 4% and 11% for devices A and B, respectively, compared to the control device at a fixed gate overdrive ($V_G - V_T$), $V_G - V_T = -0.8$ V, and $V_D = -1.0$ V. We can also extracted that V_T for the control device, device A and device B were −0.55 V, −0.51 V, and −0.48 V, respectively in the inset of Fig. 1. These results suggest that F implantation may reduce the number of border traps and control V_T [15]. By analyzing the RTN characteristics with respect to the gate voltage and the temperature, it is possible to reveal the effect of F implantation on the trap parameters within high-k dielectrics. In the RTN measurement, a distinct difference in I_D between two states under different V_G is observed as shown in Fig. 2 for the control device, devices A, B, respectively, which is responsible for carrier trapping and detrapping at a single trap

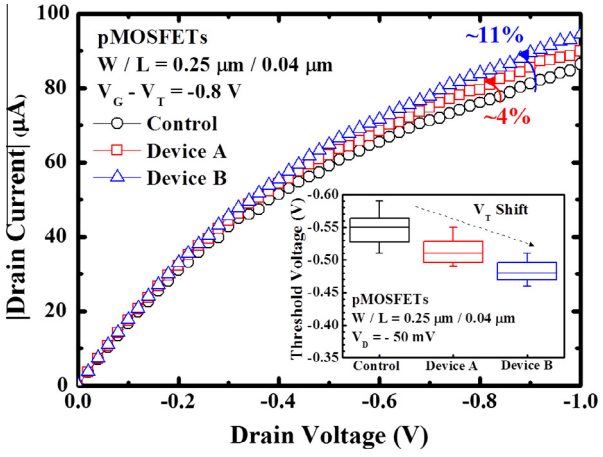

Fig. 1. Drain current versus drain voltage characteristics of all HK/MG pMOSFETs. Inset shows V_T determined from the I_D–V_G curves for the control device, devices A, B, respectively.

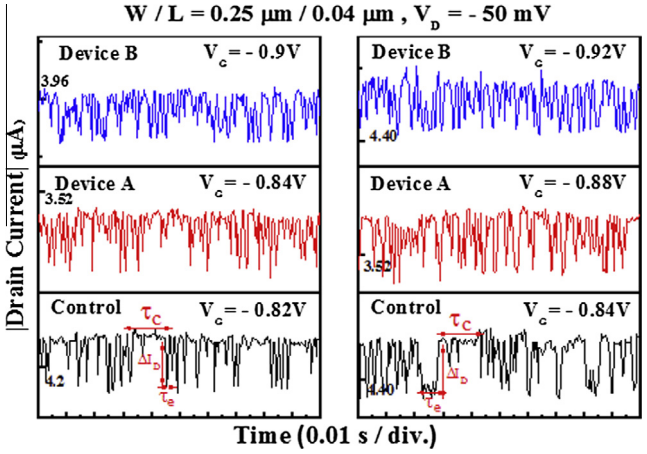

Fig. 2. Room temperatures drain current RTN for all devices with a 40-nm gate length and a 25-nm gate width as function of the gate voltage.

site and confirms the existence of RTN in all devices. The extracted mean capture time (τ_c) and mean emission time (τ_e) constant versus $V_G - V_T$ plot is shown in Fig. 3. Compared with the control device, it can be seen that τ_c and τ_e were indeed smaller for the F-implanted devices. We can also see that τ_c decreases and τ_e increases with the increase in $V_G - V_T$ for all devices. Fig. 4 shows the dependence of $\ln(\tau_c/\tau_e)$ on $V_G - V_T$ for the fabricated devices. The trap depth (X_T) from the insulator/semiconductor interface can be extracted using the following formulas [16]:

$$X_{T1} = \left(T_{ox1} + \frac{\varepsilon_{ox1}}{\varepsilon_{ox2}} T_{ox2}\right)\left(\frac{k_B T}{q}\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_{GS}} + \frac{k_B T}{q}\frac{G_m}{|I_{DS}|}\right) \Big/ \left(\frac{k_B T}{q}\frac{G_m}{|I_{DS}|} - 1\right) \quad (1)$$

$$X_{T2} = \left(T_{ox2} + \frac{\varepsilon_{ox2}}{\varepsilon_{ox1}} T_{ox1}\right)\left(\frac{k_B T}{q}\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_{GS}} + \frac{k_B T}{q}\frac{G_m}{|I_{DS}|}\right) \Big/ \left(\frac{k_B T}{q}\frac{G_m}{|I_{DS}|} - 1\right) + \left(1 - \frac{\varepsilon_{ox2}}{\varepsilon_{ox1}}\right) T_{ox1} \quad (2)$$

where X_{T1} and X_{T2} are the trap depths for the active traps located within the IL of SiO_2 and within the HK layer, respectively. T_{ox1} and T_{ox2} are the physical thicknesses of the IL and HK layers, respectively. ε_{ox1} and ε_{ox2} are the dielectric constants of SiO_2 and the HK film, respectively. As shown in Fig. 4, the dashed lines represent the linear fitted curves that are used to obtain the X_T values of all devices. The obtained values of X_T are 0.76, 0.89, and 1.51 nm for device B, device A, and the control device, respectively. The smaller X_T for the F-implanted devices indicates that the capture and emission events occur very frequently. The shifts in X_T toward the IL/Si

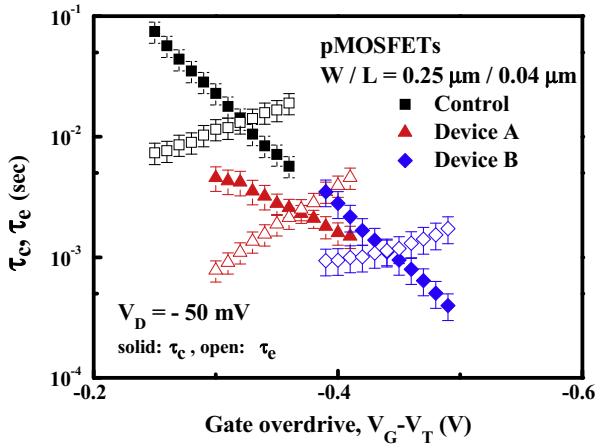

Fig. 3. Capture time (τ_c) and emission time (τ_e) of all pMOSFETs.