Solid-State Electronics 100 (2014) 1–6

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Characterization of enhancement-mode n-channel sulfur-treated InP MOSFET with Al_2O_3/TiO_2 gate oxides prepared by atomic layer deposition

Chih-Feng Yen [a], Ming-Kwei Lee [b,*]

[a] Department of Materials Science and Engineering, MingDao University, Chang Hua 52345, Taiwan, ROC
[b] Department of Electronic Engineering, Chung Yuan Christian University, Chung Li 32023, Taiwan, ROC

ARTICLE INFO

Article history:
Received 6 December 2013
Received in revised form 30 April 2014
Accepted 10 June 2014
Available online 11 July 2014

The review of this paper was arranged by Prof. E. Calleja

Keywords:
ALD
Al_2O_3
TiO_2
$(NH_4)_2S$
InP
MOSFET

ABSTRACT

Polycrystalline TiO_2 film with the thickness of 4 nm prepared by atomic layer deposition (ALD) on ammonium sulfide treated p-type InP shows a good interface quality but with slightly higher leakage current mainly resulted from the thermionic emission and grain boundary. Stacked with a high band-gap amorphous Al_2O_3 of 3 nm prepared by atomic layer deposition on TiO_2, the leakage currents are improved to 1.9×10^{-8} and 1.1×10^{-6} A/cm^2 at ±2 MV/cm. The equivalent dielectric constant of Al_2O_3/TiO_2 is about 18. The lowest interface state density is around 5.7×10^{11} cm^{-2} eV^{-1}. The fabricated enhancement-mode n-channel sulfur-treated InP MOSFET exhibits good electrical characteristics with a maximum transconductance of 135 mS/mm and electron channel mobility of 275 cm^2/V s.

1. Introduction

Owing to higher electron mobility compared with Si, much attention has been focused on indium phosphide (InP) high-speed devices. Currently, the metal–semiconductor field effect transistor (MESFET) is the main structure of InP high-speed devices. The main disadvantage of MESFET is the high leakage current of Schottky gate under the positive bias of several tenths of a volt, which severely limits the maximum drain current, the noise margin and the flexibility of the circuit design. Compared with MESFET, the gate insulating layer of metal–oxide–semiconductor field effect transistor (MOSFET) can improve these disadvantages. Gate dielectrics with low interface state density (D_{it}), and good thermal stability are essential for high quality MOSFETs. Many high-k dielectrics, such as TiO_2 [1], Al_2O_3 [2] and HfO_2 [3] are currently being explored on InP substrate. TiO_2 with a relatively high dielectric constant (k value 35–100) used as gate oxides and MOSFET with high transconductance is expected. However, the thermionic emission of low band-gap TiO_2 (3.5 eV) [4] is high. The stack of a high band-gap Al_2O_3 (9 eV) on TiO_2 can improve it.

Currently, TiO_2 films are prepared by conventional methods, such as metal–organic chemical vapor deposition (MOCVD) [4], sol–gel [5], and sputtering [6]. The atomic layer deposition (ALD) film is achieved by repeating two self-limiting depositions in an alternative sequence. A variety of high quality materials has been demonstrated by ALD, including oxides, nitrides and various metals [7]. ALD–TiO_2 and ALD–Al_2O_3 offer well-controlled thin film on atomic scale over MOCVD–TiO_2 in MOS application. The native oxides on III–V compound semiconductors will contribute high D_{it} [8]. The high D_{it} is a major concern in the development of MOSFETs. It was reported that the $(NH_4)_2S$ solution can remove the surface oxides on InP [9–11] and cover the surface with sulfur atoms to prevent further oxidization [12,13]. In this study, the enhancement-mode n-channel InP MOSFETs with ALD–Al_2O_3/TiO_2 films as gate oxides on $(NH_4)_2S$-treated InP (S-InP) substrate were characterized.

2. Experimental

Zn doped p-type InP (100) with carrier concentration of 5×10^{16} cm^{-3} was used as the substrate. The InP substrate was degreased in solvent and followed by chemical etching in a

* Corresponding author. Tel.: +886 3 2654050; fax: +886 3 2654059.
E-mail address: mklee@cycu.edu.tw (M.-K. Lee).

http://dx.doi.org/10.1016/j.sse.2014.06.026
0038-1101/

solution (H_2SO_4:H_2O_2:H_2O = 5:1:1) for 3 min and then rinsed in deionized water. After cleaning, the InP substrate was immediately dipped into the $(NH_4)_2S$ solution (10 ml of 21% $(NH_4)_2S$ solution mixed with 15 ml DI water) at 50 °C for 40 min, then rinsed in DI water and blown dry with nitrogen gas. After the $(NH_4)_2S$ treatment, the InP substrate was thermally treated at 220 °C in nitrogen atmosphere for 10 min to desorb the excess of weakly bonded sulfur for better electrical characteristics of the MOS capacitor [9] and then ready for ALD growth.

Ultrathin TiO_2 film was grown on InP by an ALD system. Tetraisopropoxytitanium ($Ti(i\text{-}OC_3H_7)_4$) kept at 24 °C was used as a Ti precursor. Nitrogen (N_2) was used as the carrier gas and its flow rate was 10 sccm. Nitrous oxide gas (N_2O) was used as an oxidizing agent and its flow rate was 100 sccm. Molybdenum was used as the oxidation-resist susceptor. The reactor pressure was kept at 5 Torr during the growth. The growth temperature and the deposition cycle were kept at 250 °C and 50. ALD–Al_2O_3 film was grown using $Al(CH_3)_3$ and H_2O as precursors. N_2 was used as the carrier gas. Stainless steel was used as the susceptor. The reactor pressure was kept at 0.1 Torr during the growth. The growth temperature and the deposition cycle were kept at 250 °C and 30. The deposition rates of TiO_2 and Al_2O_3 were about 0.8 Å and 1 Å/cycle, respectively.

For the fabrication of MOS capacitor, an In(90%)–Zn(10%) alloy was evaporated on the back side of InP substrate as an ohmic contact and annealed at 400 °C for 3 min in nitrogen atmosphere. Al was evaporated on the dielectric film as the top contact with an area of 7.07×10^{-4} cm^2. An Agilent B1500A semiconductor device analyzer and an Agilent E4980A capacitance–voltage (C–V) meter were used for current–voltage (I–V) and 1 MHz C–V characterizations, respectively. The D_{it} was derived from the high-low frequency (1 MHz-quasistatic) capacitance method. The quasistatic C–V measurement was measured by HP 4156. The dc bias is swept at 1/20 V/s and provides a sufficiently accurate D_{it} value [14].

The gate length/width of the n-channel S-InP MOSFET was 4×100 μm. After preparation of $(NH_4)_2S$ treated InP substrate, Al_2O_3/TiO_2 was sequentially deposited by ALD, and then AZ 1824 photoresist (P.R.) was spin-coated on $(NH_4)_2S$ treated InP to definite the gate region. Al_2O_3/TiO_2 was etched by inductively coupled plasma (ICP) and then the P.R. was removed to form the gate oxide. After the definition of source and drain regions with the photoresist mask, Si ions were implanted (dose of 5×10^{13} cm^{-2} at 130 keV) to achieve heavily n^+ doped source and drain. The activation of Si ions was carried out by rapid thermal annealing (RTA) at 820 °C for 20 s in a nitrogen atmosphere. A LPD-SiO_2 film of about 100 nm was deposited at 40 °C to serve as the isolation oxide. Hydrofluosilicic acid (H_2SiF_6, 3.8 M) aqueous solution saturated with silica gel and boric acid aqueous solution (H_3BO_3, 0.1 M) were used as precursors. The source/drain metal contact is formed by Al evaporation and its thickness is about 500 nm. In–Zn alloy (In 90% and Zn 10%) was evaporated on the InP back side for body metal contact and then thermally annealed at 400 °C for 3 min in N_2. The schematic structure of MOSFET is shown in Fig. 1.

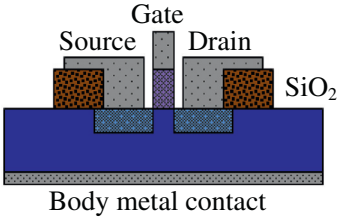
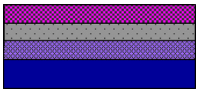


Fig. 1. Schematic structure of MOSFET.

The MOSFET process flow is as follows:

Step 1

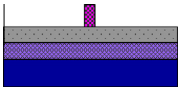
ALD–Al_2O_3/TiO_2 gate oxides on $(NH_4)_2S$-treated InP were deposited, then, followed by Al gate deposition and photoresist coating



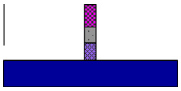
P.R./Al/Al_2O_3/TiO_2/were deposited on $(NH_4)_2S$ treated InP

Step 2

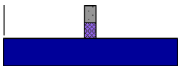
The gate region was defined. The Al_2O_3/TiO_2 was etched by inductively coupled plasma (ICP) with a gas mixture of C_4F_8, SF_6 and O_2. Then, the P.R. was removed to preserve the gate oxide and gate metal



P.R. was defined by photolithograph



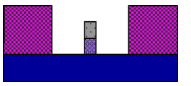
Al_2O_3/TiO_2 was etched by ICP



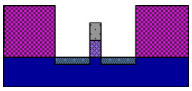
P.R. was removed to form the gate oxide and gate metal

Step 3

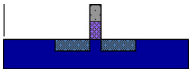
Source and drain windows for ion implantation were defined



Define source and drain windows



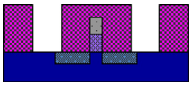
Ion implantation and activated by RTA



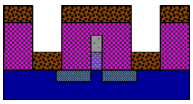
P.R. removed by acetone

Step 4

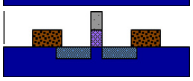
Isolation oxide regions for LPS–SiO_2 deposition were defined



P.R. coated



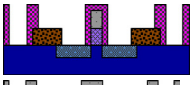
SiO_2 deposited



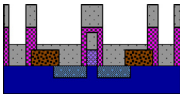
P.R. removed with acetone

Step 5

Al deposition was defined for source/drain metal contacts



Source/drain metal contacts defined



Source/drain Al metal contacts deposited