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# Performance of AlGaN/GaN MISHFET using dual-purpose thin $Al_2O_3$ layer for surface protection and gate insulator

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ABSTRACT

In this work, we have investigated a role of a thin $Al_2O_3$ layer in AlGaN/GaN MISHFET by characterizing the variation of the sheet resistance of the 2DEG channel layer. The $Al_2O_3$ layer, varying the thickness from 0 to 10 nm, was utilized as the gate insulator of the device as well as the surface protection layer during RTP for ohmic contact formation. After RTP, the 2DEG channel layer without the $Al_2O_3$ layer was rapidly degraded by increasing the sheet resistance of the layer to 1360 Ω/□ from the sheet resistance of 400 Ω/□ of the as-grown sample. The degradation was still observed even when 1.5 nm-thick $Al_2O_3$ layer was used. However, the sheet resistances of the devices remained constant with slightly decreased value from that of the as-grown sample when the thickness is larger than 3 nm, which indicates that the 3 nm-thick $Al_2O_3$ layer well protects the AlGaN surface above the 2DEG channel during RTP. The slight decrease in sheet resistance is probably because some acceptor-like states existing at AlGaN surface become neutralized and hence the 2DEG density increases. The $Al_2O_3$ layer was not removed for proceeding the fabrication of AlGaN/GaN MISHFET, but rather used as a gate dielectric, which simplifies the device fabrication eliminating the additional deposition steps for the gate dielectric. The threshold voltage of the device, investigated in this work, was increased to the negative direction with increasing the thickness of $Al_2O_3$ layers while the transconductance was decreased. The best performances were obtained from the device with 8 nm-thick $Al_2O_3$ layer, exhibiting very low gate leakage current of $10^{-9}$ A/mm with subthreshold swing (SS) of 80 mV/dec and very high $I_{on}/I_{off}$ ratio (>9 orders).


## 1. Introduction

AlGaN/GaN-based heterojunction field-effect transistors (HFETs) have been reported as one of the most promising devices for high-power and high-frequency applications due to excellent material properties of nitride-based compounds such as wide bandgap, high breakdown voltage and high two-dimensional electron gas (2DEG) density [1–4]. In general, an AlGaN layer with optimized thickness is required to improve the device performances of AlGaN/GaN HFETs [5,6]. However, when the AlGaN layer is exposed to high temperature process such as rapid thermal process (RTP), the surface of the layer can be easily damaged, which results in the increase of sheet resistance of 2DEG channel layer [7,8]. Therefore, during high temperature RTP, an effective surface protection layer such as relatively thick $SiO_2$ or $Si_3N_4$ layer is necessary for the fabrication of high performance AlGaN/GaN HFET.

In this work, we have investigated the thin $Al_2O_3$ dielectric layer which is used as an excellent gate dielectric in AlGaN/GaN MISHFETs [9] and as a possible surface protection layer instead of thick $SiO_2$ or $Si_3N_4$ layer as shown in Fig. 1. The use of the thin $Al_2O_3$ layer simplifies the fabrication of the AlGaN/GaN MISHFET because an additional deposition step for gate dielectric layer is not required.

## 2. Experiment

The 17 nm-thick AlGaN/GaN heterostructure was grown on sapphire (0001) substrate by metal organic chemical vapor deposition (MOCVD) at 1070 °C. Hall measurement for the as-grown heterostructure showed the electron mobility of 1900 $cm^2/V\,s$, the sheet electron concentration of $8 \times 10^{12}/cm^2$, and the sheet resistance of 400 Ω/□.

Mesa etching was carried out to define the active region by transformer-coupled-plasma reactive ion etching (TCP-RIE) using a $BCl_3/Cl_2$ gas mixture. To protect the AlGaN surface from high

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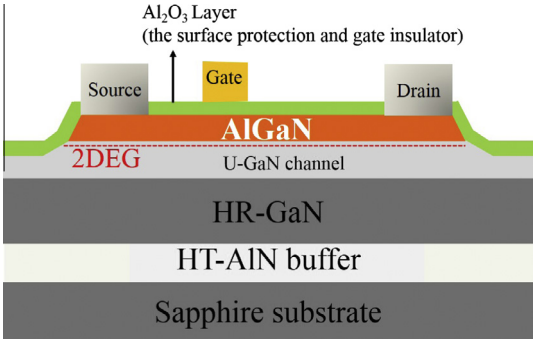


**Fig. 1.** Schematic structure of AlGaN/GaN MISHFET fabricated with thin $Al_2O_3$ layer.

temperature RTP for ohmic contact formation, thin $Al_2O_3$ dielectric layer (thickness of 0, 1.5, 3, 5, 8, and 10 nm) was then deposited with a deposition rate of 0.7 Å/cycle at 450 °C by using plasma-enhanced atomic layer deposition (PEALD). The use of thin $Al_2O_3$ dielectric layer is very important because it can be directly utilized as gate insulators, which simplifies the fabrication of the AlGaN/GaN MISHFET because there is no need of removing the layer after RTP and re-deposition of the gate insulator. For the ohmic contact formation, the $Al_2O_3$ layer on the source/drain region was etched away and metal layers (Si/Ti/Al/Ni/Au) were deposited, followed by two-step RTP carried out firstly at low temperature of 500 °C for 20 s and subsequently at higher temperature of 800 °C for 30 s in $N_2$ ambient. Finally, Ni/Au gate metal was deposited. The gate length and width of the fabricated AlGaN/GaN MISHFETs were 3 and 100 μm, respectively. The variation of the contact resistance and sheet resistance of the device after RTP were characterized by using transmission line method (TLM) [10].

## 3. Results and discussion

Fig. 2 shows the averaged sheet resistances of samples versus the thickness of the $Al_2O_3$ protection layer after RTP, which were extracted with the TLM measurement. When no protection layer was applied, high temperature annealing during RTP affected the surface of the AlGaN layer and hence the sheet resistance of the heterostructure became increased to 1360 Ω/□ from the value of ~400 Ω/□ of the as-grown sample. The sheet resistance of the sample was also increased to ~678 Ω/□ even when 1.5 nm-thick $Al_2O_3$ protection layer was deposited on the AlGaN surface, which indicates that 1.5 nm-thick $Al_2O_3$ layer is not sufficient to protect the AlGaN surface. For the thickness larger than 3 nm, however, the sheet resistances of the samples were not increased, but rather slightly decreased compared with that of the as-grown sample. The decrease in sheet resistance is probably resulted from the fact that the $Al_2O_3$ layer not only prevents the surface being damaged during RTP, but also effectively neutralizes the acceptor-like states which is existed on the AlGaN surface. The neutralization of the acceptor-like states is responsible for the increase in the 2DEG concentration [11,12]. The averaged ohmic parameters after RTP were summarized in Table 1.

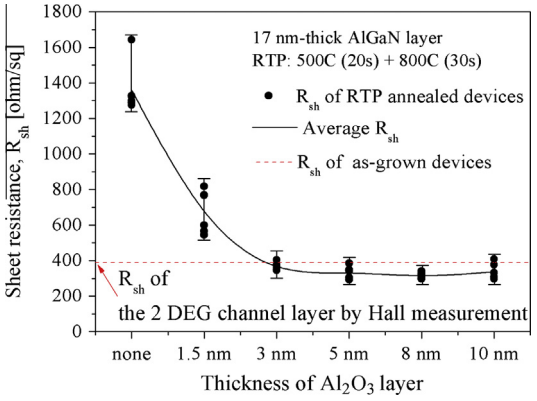


**Fig. 2.** Averaged sheet resistances of the variation of the thickness of $Al_2O_3$ layer after annealing.

Fig. 3(a) shows the static DC characteristics of all fabricated AlGaN/GaN (MIS)HFETs with the $Al_2O_3$ thickness of 0 (device A), 1.5 (B), 3 (C), 5 (D), 8 (E), and 10 nm (F) respectively. The threshold voltages of the devices were shifted from −0.9 to −5 V with increasing the thickness of the $Al_2O_3$ layer as following Eq. (1).

$$V_T = -\frac{Q_\pi(\text{net})\cdot d_{\text{eff}}}{\varepsilon} + \left(\phi_b - \frac{\Delta E_C}{q}\right) \tag{1}$$

where $Q_\pi$(net) ($Q_\pi$(net) = $Q_\pi$(AlGaN) − $Q_\pi$(GaN)) is the sum of the polarization charge contributions from the AlGaN layer and the GaN layer, $\varphi_b$ is the metal-semiconductor barrier height, $\Delta E_C$ is the conduction band discontinuity, and $d_{\text{eff}}$ is the effective barrier thickness.

On the other hand, the maximum transconductances of all devices became decreased with increasing the thickness of $Al_2O_3$ layer as shown in Fig. 3(b). This is because thicker $Al_2O_3$ layer

**Table 1**
The average parameters extracted from TLM.

| $Al_2O_3$ thickness | None | 1.5 nm | 3 nm | 5 nm | 8 nm | 10 nm |
|---|---|---|---|---|---|---|
| Contact resistivity ($\rho_c$) (μ Ω cm$^2$) | 23 | 2.96 | 4.25 | 15 | 5.33 | 4.5 |
| Contact resistance ($R_c$) (Ω mm) | 0.20 | 0.20 | 0.35 | 0.56 | 0.34 | 0.35 |
| Sheet resistance ($R_{sh}$) (Ω/□) | 1360 | 678 | 367 | 330 | 316 | 337 |

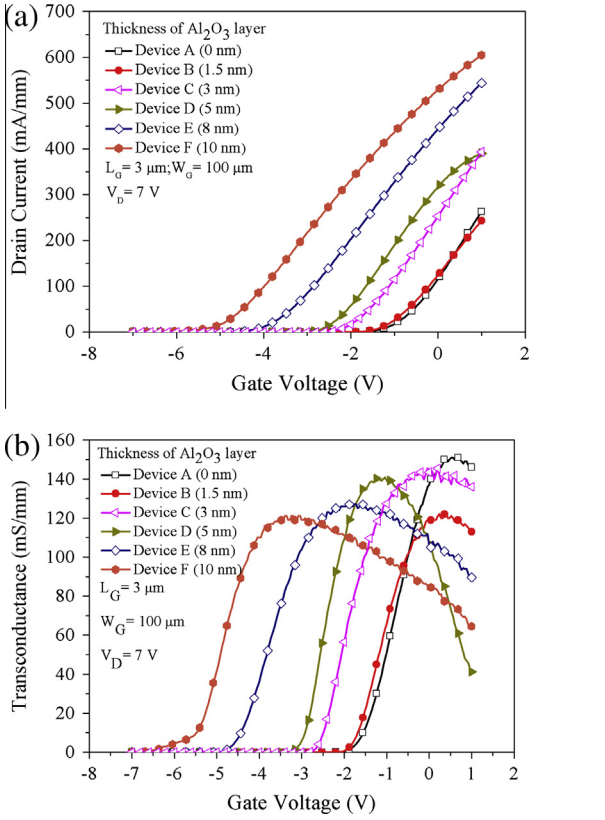


**Fig. 3.** (a) $I_D$–$V_G$ characteristics and (b) $g_m$–$V_G$ characteristics of all devices as functions of gate bias with varying the $Al_2O_3$ thickness.