Solid-State Electronics 100 (2014) 39–44

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Incremental resistance programming of programmable metallization cells for use as electronic synapses

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ARTICLE INFO

Article history:
Received 1 March 2014
Received in revised form 25 June 2014
Accepted 3 July 2014
Available online 22 July 2014

The review of this paper was arranged by Dr. Y. Kuk

Keywords:
Chalcogenide
PMC
Resistive memory
ReRAM
Synapse

ABSTRACT

In this work, we investigate the resistance switching behavior of Ag–Ge–Se based resistive memory (ReRAM) devices, otherwise known as programmable metallization cells (PMC). The devices studied are switched between high and low resistive states under externally applied electrical bias. The presence of multiple resistive states observed under both dc and pulse voltage application makes these devices promising candidates for use as electronic synapses in neuromorphic hardware implementations. Finally, the effect of varying pulse voltage magnitude and width on the change in resistance is observed through measurement.

1. Introduction

Resistive random access memory (ReRAM) devices have been the subject of extensive research as they constitute an alternative to charge-based non-volatile memory technologies, such as flash memories [1–3]. In this paper, we concentrate on a particular class of cation based ReRAM technology known as programmable metallization cell (PMC) or alternatively as conductive bridge random access memory (CBRAM). Low switching energy and ease of integration into standard CMOS processes are among the features that make PMCs suitable for memory applications [4,5]. In memory, PMC devices behave primarily as switches, alternating between high and low resistance states. However there is growing interest in exploring the possibility of changing the resistance of such devices in a more gradual manner. The capability of programming multiple resistance states is necessary for using these devices in neuromorphic hardware [6] which aims to mimic the architecture and functionality of the biological brain.

In this work we consider silver (Ag)–germanium selenide ($Ge_{30}Se_{70}$) based PMC devices. Similar PMC devices have been considered mainly as memory storage elements until now [7]. Previously pulse-based programming and characterization on germanium sulfide (GeS_2) based PMCs have focused on investigating the kinetics of PMC resistance change through the application of voltage pulses [8]. Here we specifically investigate the capability of setting multiple resistance levels in the PMC device through both DC and transient voltage pulse application and experimentally demonstrate gradual resistance programmability in this technology.

The brain consists of a massively parallel network of millions of computing units called neurons interacting with each other via conductive pathways called synapses [9]. There has been long-standing research interest in developing artificial brain-like electronic systems with the ability to learn and adapt [10,11] to provide an alternative to the existing Von Neumann computing paradigm. This learning capability in biological brains is believed to originate from the ability to modulate the conductive strength of their synaptic pathways in a continuous manner based on voltage spikes generated by the neurons in response to input sensory signals [12]. Since the synapses vastly outnumber the neurons, using a single ReRAM device as an electronic synapse should reduce power and area consumption vastly compared to CMOS based circuits. Previously, oxide based [13] and amorphous silicon based [14] ReRAM as well as phase change memory (PCM) devices [15] have been used to demonstrate the property of continuous

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http://dx.doi.org/10.1016/j.sse.2014.07.002
0038-1101/

resistance programmability analogous to the biological synaptic strength modulation. The demonstration of this gradual programming property of PMC devices in this work along with its ease of back end of line (BEOL) integration makes the PMC a strong candidate for use in hybrid CMOS-ReRAM based neuromorphic circuit implementations [16,17].

2. Material and methods

The PMC is a two terminal resistive memory device with a metal–electrolyte–metal (MEM) structure consisting of a layer of thin film electrolyte, in this case, chalcogenide glass (ChG), in between a silver (Ag) anode (active electrode) and a nickel (Ni) cathode (inert electrode). An illustration of a PMC device cross-section is shown in Fig. 1(a) and a micro photograph showing top view of a 10 μm device is shown in Fig 1(b). The ChG (amorphous $Ge_{30}Se_{70}$) and Ag layers are deposited by thermal evaporation into an etched via. In order to define the via layer and the bottom electrode, a photo resist film of 1 μm thickness was spun using a standard resist spinner and then the sample was soft baked to remove additional solvent from the photoresist. This was followed by a lithography step in which the samples were exposed using via mask. The samples were subsequently developed and hard baked to make the resist more durable. Then a buffered oxide etch was performed. Finally the remaining resist was removed using acetone [18]. The Ag deposit is then subjected to a UV light exposure (λ = 324 nm, E = 3.82 eV) for 1 h at a power density of 10 mW/cm^2. This induces Ag photo-doping into the ChG film, which primes the device for resistance switching. After photo-doping, additional Ag is deposited to act as the anode. The last step in PMC fabrication involves annealing at 120°C for 20 min. All tests were performed on devices with 5 μm and 10 μm diameter vias.

3. Theory

In conventional operation, the PMC acts a nonvolatile resistive storage element. Reduction in resistance occurs when a conductive filament (CF) is formed in response to a positive voltage applied to the Ag anode. The electrical stimulus induces oxidation at anode and the subsequently released Ag^+ ions transport through ChG film to the cathode where reduction takes place. The continuation of these redox processes leads to the formation of an Ag rich conductive filament across the film. Once a conductive bridge forms between the electrodes, the initial high resistance state (HRS) of the PMC changes to a low resistance state (LRS) which is defined by the CF resistance. After the formation of this bridging filament, if the positive bias continues to be applied, the diameter of the filament gradually increases which further decreases the PMC resistance. Under reverse bias, the filament gradually shrinks until the contact with the top electrode has dissolved. This marks the transition back to the HRS. A schematic representation of the transition between the two resistive states is shown in Fig. 2.

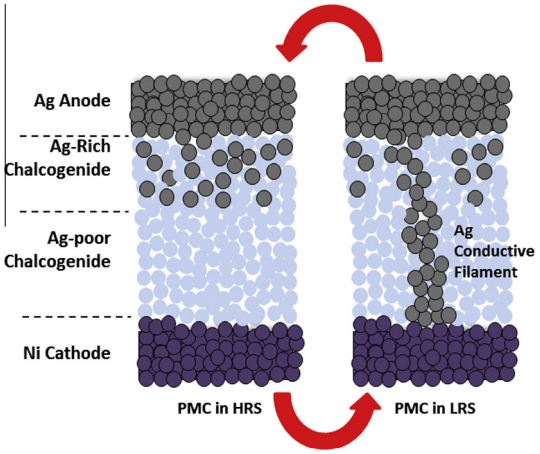

Fig. 2. Schematic representation of high resistance states (HRS) and low resistance state (LRS).

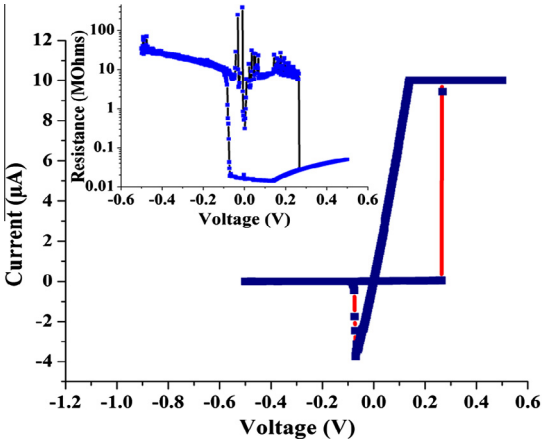

Fig. 3. A typical measured DC *I–V* characteristics of a PMC device (5 μm diameter) with a 10 μA compliance current, with the corresponding resistance vs. voltage plot (semi-log scale) shown as inset.

A typical current–voltage (*I–V*) characteristic plot for a PMC device is shown in Fig. 3. In these devices, the positive switching voltage threshold ('write' threshold for the HRS to LRS transition) was close to 250 mV, while the negative voltage threshold ('erase' threshold for the LRS to HRS transition) was around −100 mV.

4. Results and discussion

4.1. Resistance programming in quasi static (DC) mode

The existence of multiple programmable resistance states in PMC devices was experimentally verified by performing DC voltage

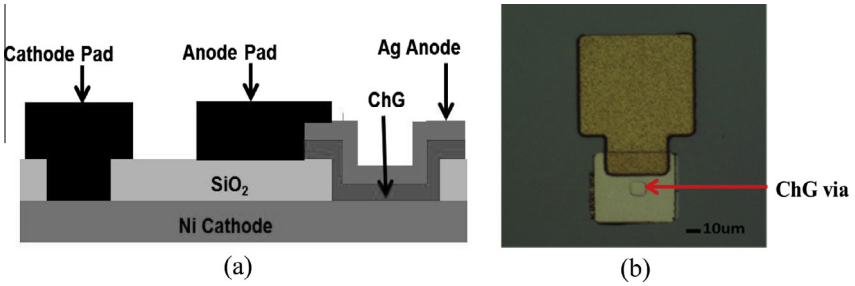

Fig. 1. (a) Programmable metallization cell (PMC) cross section showing Ag anode, photo-doped ChG (chalcogenide $Ge_{30}Se_{70}$) via and Ni cathode. (b) Micro photograph of top view of a 10 μm diameter PMC device.