



Letter

Performance improvement of normally off AlGaIn/GaN FinFETs with fully gate-covered nanochannel



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ABSTRACT

Normally-off AlGaIn/GaN FinFETs have been fabricated by fully covering the nanochannel region with a metal gate. Removing the source/drain extensions (gate underlap regions) greatly decreases the access resistance of the device, which results in an order of magnitude higher on-current and transconductance. As compared with earlier HEMT FinFETs, where the nanochannel is only partially covered by the gate, the carrier trapping at the surface and in the buffer layer is effectively reduced, improving the gate and the drain lags.

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1. Introduction

AlGaIn/GaN-based FinFETs with nanowire structures have been recently fabricated [1–5]. They exhibited promising performance due to the 3-dimensional (3-D) gate configuration which greatly improves the gate control of the nanosize channel. For example, Zimmermann et al. [1], Lu et al. [2], and Ohi and Hashizume [5] showed very low subthreshold slope (SS) and high maximum drain current ($I_{d,max}$) can be obtained from AlGaIn/GaN nano-devices.

In addition, as suggested and demonstrated by several groups [1–5], normally-off operation with positive threshold voltage (V_{th}), which is very important for power switching applications, can be achieved by reducing the fin width to less than 100 nm. From a device-processing viewpoint, the simplicity of this approach (fin size reduction) is very attractive. By comparison conventional planar AlGaIn/GaN HFETs or MISHFETs require additional technology steps to achieve a normally-off operation [6–10].

The HEMTs and FinFETs fabricated to date featured gate underlap regions. In this paper, we have fabricated, characterized, and compared normally-off AlGaIn/GaN nanochannel FinFETs with partially-covered (Fig. 1(a)) and fully-covered (Fig. 1(b)) gate

structure. The latter device exhibits a positive V_{th} and significantly enhanced performances, compared to more usual AlGaIn/GaN transistor (normally-off HFETs or MISHFETs [6–10]) with either planar or underlap FinFET architecture.

2. Growth and device fabrication

The AlGaIn/GaN heterostructure was grown on sapphire (0001) substrates by metal–organic chemical vapor deposition (MOCVD). The detailed growth processes, epitaxial structures, and layers thickness are the same as those of conventional AlGaIn/GaN HFETs. The two-dimensional electron gas (2DEG) density ($8.8 \times 10^{12} \text{ cm}^{-2}$) and electron mobility ($\sim 1500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) at the AlGaIn/GaN heterointerface were measured by Hall effect. The fin-shaped active region of the device, with fin height of 120 nm and variable width (from 60 to 120 nm), was defined by electron-beam lithography followed by transformer-coupled plasma-reactive ion etching (TCP-RIE). The etching depth was controlled such as to remove the 2DEG in the trench regions. In order to smooth the surface and remove the plasma damage from the etched GaN surface, surface treatment was directly followed in a tetramethyl ammonium hydroxide (TMAH) solution for 30 min (25% solution at 85 °C) [4,9,11]. The gate-dielectric consisted of 20 nm-thick Al_2O_3 deposited by atomic layer deposition at 450 °C. After contact hole

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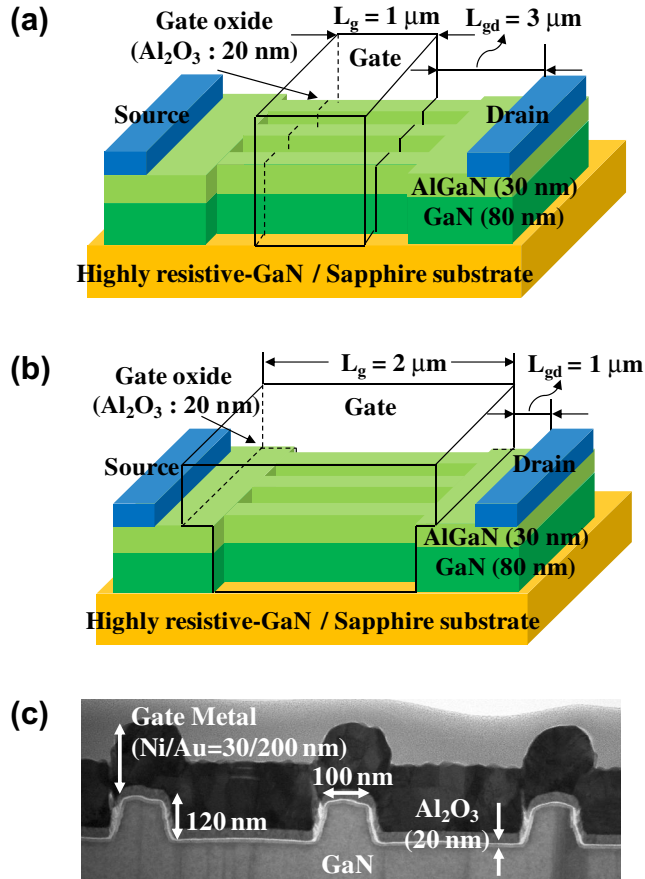


Fig. 1. Schematic illustrations of nanochannel AlGaIn/GaN FinFETs with (a) partially gate-covered nanochannel (reference device) and (b) fully gate-covered nanochannel (proposed device). The gate insulator is 20 nm-thick Al_2O_3 (not shown). (c) The cross-sectional TEM image. Both devices have $H_{\text{fin}} = 120$ nm, $W_{\text{fin}} = 60$ –120 nm, and 3 parallel fins.

opening for the source and drain, Ti-based ohmic-contact metals were deposited using an electron-beam evaporator, followed by rapid thermal annealing (RTP) at 900 °C for 30 s in nitrogen ambient. Finally, Ni/Au was deposited as the gate metal. Fig. 1(a) and (b) show the schematic configurations for the AlGaIn/GaN FinFETs with partially gate-covered nanochannel (reference device) and fully gate-covered nanochannel (proposed device free of gate underlap). The reference device (partially gated) has gate length of $L_g = 1$ μm and gate metal-to-drain pad distance of 3 μm. The corresponding length and distance for the proposed device (fully gated) are 2 and 1 μm, respectively. Image of the cross-sectional transmission electron microscopy for the fabricated device with multi-channel array is shown in Fig. 1(c).

3. Results and discussion

The threshold voltage, V_{th} , was defined as the gate voltage at 1% of maximum drain current, which roughly corresponds to the value obtained from the intercept of the linear $\sqrt{I_{\text{ds}}}$ vs. V_{gs} curves in saturation region. Both devices exhibit normally-off operation with $V_{\text{th}} \approx 2.1$ V at $V_{\text{ds}} = 5$ V, as shown in the $I_{\text{ds}}-V_{\text{gs}}$ curve of Figs. 2(a) and 3(a), even though they have a horizontal 2DEG channel near the top of the fin. The normally-off operation in these nanostructured devices is due to the depletion (pinch-off) of the 2DEG channel at $V_{\text{gs}} < 0$, caused by the fringing field from the sidewall sections of the gate [1–5]. As a matter of fact, in our wider fins the lateral fringing field is no longer able to fully deplete the 2DEG and V_{th} becomes negative; this implies that in narrow

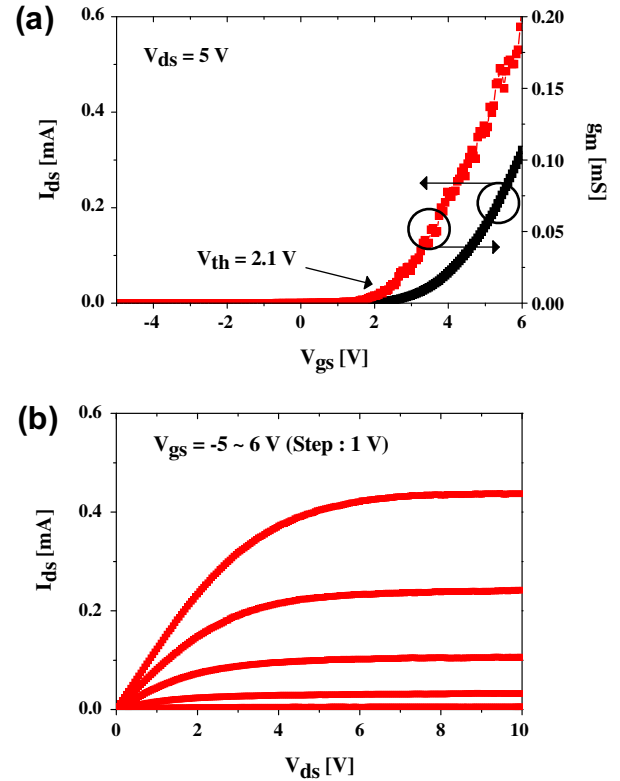


Fig. 2. (a) Transfer curve of the reference device at $V_{\text{ds}} = 5$ V and (b) corresponding $I_{\text{ds}}-V_{\text{ds}}$ characteristics. $L_g = 1$ μm, $W_{\text{fin}} = 60$ nm, 3 fingers.

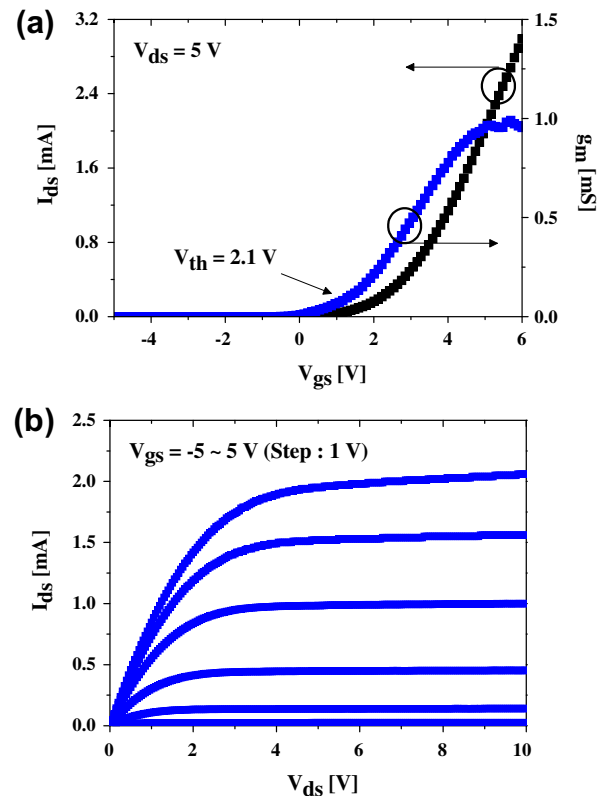


Fig. 3. (a) Transfer curve of the newly proposed underlap-free device at $V_{\text{ds}} = 5$ V and (b) $I_{\text{ds}}-V_{\text{ds}}$ characteristics. $L_g = 2$ μm, $W_{\text{fin}} = 60$ nm, 3 fingers.

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