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Comparative studies on electrical bias temperature instabilities of In–Ga–Zn–O thin film transistors with different device configurations

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ABSTRACT

We investigated the effect of positive bias temperature stress (PBTS) on the device stabilities of In–Ga–Zn–O thin film transistors with bottom gate and top gate structures. Under the PBTS conditions at the gate voltage of +20 V and the temperature of 60 °C, the turn-on voltage experienced a negative shift of −1.5 V for the top gate device, while a larger positive shift of 3.0 V was observed for the bottom gate device. From the variations in transfer characteristics at various temperatures and the discussions on the thermal activation energy, it was suggested that these different behaviors of two devices originated from interface trap densities caused by the plasma damage and the pinning of Fermi energy level for the bottom and top gate devices, respectively. It was very encouraging that the variation of the turn-on voltage could be minimized when the top gate device was fabricated to have a very controlled interface.

1. Introduction

Technical potentials of oxide semiconductor thin-film transistors (TFTs) have been aggressively exploited as promising backplane devices for large-area and high resolution flat-panel displays such as active-matrix organic light-emitting diode (AMOLED) and active-matrix liquid crystal display (AMLCD) [1–4]. For the full-scale commercialization of these panels, device reliabilities of oxide TFT backplanes should be carefully controlled with their high performances including high field-effect mobility and superior uniformity. Amorphous In–Ga–Zn–O (α-IGZO) is one of the most typical material compositions of the oxide semiconductors and have been mainly employed for the fabrication of oxide TFTs [5–7]. So far, device reliability characteristics of α-IGZO TFTs have been investigated under various stress conditions such as negative/positive gate bias stress (NBS/PBS) [8,9], negative gate bias illumination stress (NBIS) [11,12,10], gate bias temperature stress (BTS) [13,14], drain bias stress [15,16], constant current stress [17], and ambient effects [18–21], in which instability mechanisms at various stress situations and suitable strategies for stability improvements have been actively discussed. Typical observations could be classified into two kinds of feasibilities: (1) hole trapping into the gate insulator bulk and/or at the interface between the gate insulator and oxide channel layer, (2) changes of carrier density in the active channel due to the additional state creation. Related discussions and investigations on these issues are now on process and definite conclusions are still controversial. Furthermore, these stability characteristics of oxide TFTs were observed to be very sensitively affected by the process methodologies and device structures [22–24]. Actually, we previously demonstrated an excellent NBS and NBIS characteristic of the α-IGZO TFT by introducing the interface protection layer (PL) between the gate insulator and active channel layers [25]. On the other hand, most devices evaluated in many literatures were fabricated to be bottom gate (BG) structures. Gate insulators of the BG oxide TFTs are easy to be damaged during the sputtering process of IGZO channel layer, even though they can be manufactured by using conventional fab facilities for the a-Si TFTs. Consequently, the top gate (TG) structure can be also a promising alternative to obtain both high performance and excellent stability for the practical applications of oxide TFT backplanes. From these viewpoints, systematic comparative studies on device reliabilities between the BG and TG-structured α-IGZO TFTs would provide some very interesting and important insights to understand the stability issues of oxide TFTs. In this letter, two types of BG and TG α-IGZO TFTs were fabricated and their positive gate bias temperature stabilities (PBTS) were investigated and compared. The degree of instabilities and possible mechanisms were totally different between two types of devices. From the obtained results, it was elucidated that the

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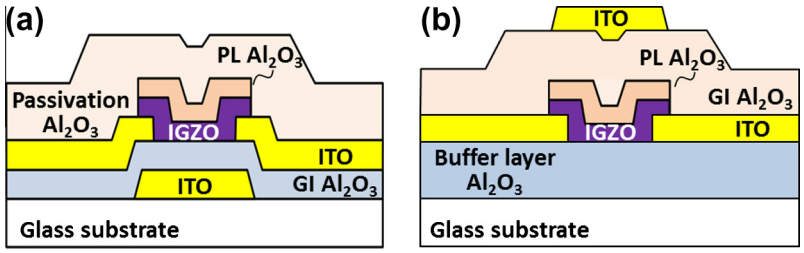

Fig. 1. Schematic cross-sectional diagrams of the fabricated (a) bottom-gate and (b) top-gate α-IGZO TFTs. All the electrodes were patterned by ITO layers. The first Al_2O_3 layers correspond to the gate insulator and buffer layers for the bottom- and top-gate TFTs, respectively. The second Al_2O_3 layers are worked as the passivation and gate insulator layers for both TFTs, correspondingly.

appropriate design scheme for the device structure and fabrication process are very important to realize highly reliable α-IGZO TFTs.

2. Experimental details

α-IGZO TFTs with BG and TG structures were fabricated with following procedures. For the first step, a 150 nm thick indium-tin-oxide (ITO) thin film was deposited by radio-frequency (rf) magnetron sputtering and patterned into gate electrodes on the glass substrate of BG device. Al_2O_3 films with thickness of 185 nm were prepared via atomic layer deposition (ALD) method using an Al precursor of trimethylaluminium and water vapor at 150 °C for both TFTs, which correspond to the gate insulator and buffer layers for the BG and TG devices, respectively. The second ITO layers were deposited and patterned into source/drain (S/D) electrodes. 25 nm thick α-IGZO active layer was formed by rf sputtering of a single IGZO (In:Ga:Zn = 1:1:1 atomic ratio) target as active channel layers of both devices. The deposition process was carried out in a mixed atmosphere of Ar and O_2 [Ar:O_2=4:1] at room temperature.Al_2O_3 layers with thickness of 9 nm were subsequently formed by ALD method at 200 °C as interface PLs to protect underlying IGZO active layers from chemical damages during the channel patterning process [25]. For this reason, the PL was introduced right before the active patterning process for both TG and BG devices. Then, 176 nm thick Al_2O_3 layers were prepared on the patterned active channels as passivation and main gate insulator 150 °C for BG and TG devices, respectively. The last ITO film was deposited and patterned into gate electrodes of TG device. Fig. 1 (a) and (b) illustrates the cross-sectional schematic diagrams of the fabricated BG and TG devices, respectively. The fabricated devices were finally annealed at 250 °C for 2 h to guarantee sound device behaviors, which is generally performed for the oxide TFTs. The electrical characteristics of the TFTs were evaluated using a semiconductor parameter analyzer (Agilent B1500A) in a dark box. The PBTS stress tests for the devices were carried out on a hot chuck equipped on the probe positioning system from room temperature to 100 °C in an air ambient.

3. Results and discussions

Fig. 2(a) and (b) shows the drain current (I_{DS})-gate voltage (V_{GS}) transfer curves for the fabricated BG and TG devices, respectively. The measurements were successively carried out at two drain voltages (V_{DS}'s) of 0.1 and 10.1 V at forward and reverse sweeps of V_{GS} for each device with the gate width (W) and length (L) of 40 and 20 μm, correspondingly. For the BG device, the field effect mobility (μ_{fe}), threshold voltage (V_{th}), turn-on voltage (V_{on}), which was defined as the voltage when the I_{DS} launched from the off-current level, and subthreshold swing (SS) were measured to be 15.0 $cm^2 V^{-1} s^{-1}$, 0.68 V, −0.37 V, 0.09 V/dec, respectively. The same device parameters of the TG device were obtained to be 14.9 $cm^2 V^{-1} s^{-1}$, 0.38 V, −0.49 V, and 0.08 V/dec, respectively. Both devices exhibited excellent device behaviors and there were not so marked differences between the devices. Irrespective of these good characteristics, it is important to check the electrical bias and/or temperature instabilities of the devices. In order to confirm the variations in PBS stabilities of the BG and TG devices, a V_{GS} of +20 V was applied to the gate terminals for 10^4 s at room temperature and corresponding transfer curves (linear and logarithmic) were measured at V_{DS} of 10.1 V, as shown in Fig. 2(c) and (d), respectively. As can be seen in figures, it can be very noticeable that the characteristics did not experience any remarkable instability for both devices. After the PBS stress for 10^4 s, the μ_{fe},V_{on}, and SS values of BG and TG devices were measured to be 16.3 and 16.2 $cm^2 V^{-1} s^{-1}$, −0.26 and −0.32 V, and 0.10 and 0.10 V/dec, respectively. Although small positive shifts in V_{on} were observed, both fabricated devices showed good immunity to the PBS stress at room temperature. On the other hand, for the cases of NBS and NBTS evaluations, there were no marked variations in their transfer characteristics for 10^4 s and no marked differences between the BG and TG devices. If any electron–hole pair would not be generated by a photon energy with illumination effect, as expected during the NBTIS test, undesirable hole trapping caused by the NBTS would not be a critical issue for the well-fabricated IGZO TFTs.

The next evaluations were carried out at 60 °C, in which a V_{GS} of +20 V was also applied to the gate terminals for 10^4. Fig. 3(a) and (b) shows the variations in I_{DS}–V_{GS} transfer characteristics for the fabricated BG and TG devices with the lapse of stressed time, respectively. The increase in temperature under the positive gate bias made big differences in device characteristics from those tested at room temperature as well as between the BG and TG devices. Fig. 3(c) and (d) summarize variations in V_{on}, SS, and μ_{fe} for both devices with the evolution of PBTS test time, respectively. The most marked difference was that the instability in V_{on} of the BG device was much larger than that of the TG device. The positive shift in V_{on} under PBTS condition without marked degradation of the μ_{fe} and SS can be generally explained to be due to the electron trapping into the bulk region of gate insulator and/or interface between the gate insulator and active channel layers [8]. It can be considered that a large ΔV_{on} of more than 3.0 V for the BG device was caused by some plasma-induced mechanical damages to the gate insulator during the sputtering process for the IGZO formation. Especially, considerable increase in trap sites at the interface may greatly influence on the electron trapping mechanism at an elevated temperature. On the other hand, it is also very important to note that the instability of the TG device appeared to be some negative shift of the V_{on}, which was completely different from the general trend observed for the PBTS condition. This anomalous behavior confirmed for our TG device suggests that its PBTS instability could be caused by other possibilities than the electron trapping mechanism. We believe that this negative shift in V_{on} under PBTS can be observed for only limited devices fabricated with