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Impact of electrical stress on the electrical characteristics of 2 MeV electron irradiated metal-oxide-silicon capacitors with atomic layer deposited Al_2O_3, HfO_2 and nanolaminated dielectrics

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ABSTRACT

In this work, the impact of electrical stress on the electrical characteristics of 2 MeV electron irradiated metal-oxide-silicon capacitors with atomic layer deposited (ALD) high permittivity (high-k) dielectric layers of Al_2O_3, HfO_2 and a nanolaminate of them is evaluated. The aim is to investigate the susceptibility to electrical stress of the radiation effects created in irradiated MOS structures, paying especial attention to any possible interaction between the radiation-induced damage and the subsequent electrical stress degradation. For this study, MOS capacitors with a nominal dielectric physical thickness of 10 nm (equivalent oxide thickness (EOT) between 3 nm and 7 nm) on different p-type and n-type silicon substrates were investigated. An exponentially increasing stress current was forced to flow in accumulation through the different dielectric layers, registering the evolution of gate voltage versus stress time until dielectric breakdown occurred. Capacitance–voltage characteristics of the different irradiated and non-irradiated structures are analyzed as a function of electrical stress. Different charge trapping behaviors and significant polarity dependence in interface state generation are observed for the dielectric layers subjected to substrate and gate injections. No clear interaction between radiation and electrical stress damages is noticed under substrate injection (n-type samples). However, higher negative charge trapping near the metal/dielectric interface is registered for the irradiated Al_2O_3 and nanolaminate layers subjected to gate injection and, in the case of the most irradiated samples, the radiation-induced interface states damage is found to dominate against the damage generated in early stages of the electrical stress.

1. Introduction

During the last decade a number of high permittivity (high-k) dielectrics have been investigated as candidates to replace the SiO_2 as gate dielectric in complementary metal–oxide-semiconductor (CMOS) technologies, being Al_2O_3 and HfO_2 among the most studied ones [1,2]. Apart from CMOS technologies, high-k dielectrics are also of strong interest for a wide range of micro/nanoelectronics applications, including, resistive random access memories (ReRAM) [3,4], emerging nanodevices [5,6], organic light emitting diodes [7], high-efficiency silicon solar cells [8], and for a variety of microelectromechanical systems [9]. In all these applications, high-k dielectric layers with typical thickness from a few nanometers to some tens of nanometers are of interest. The requirements of large area uniformity, conformality and accurate thickness control of the dielectric layers can be achieved by means of atomic layer deposition (ALD), a technique with a great potential for all the above applications. Moreover, a good advantage of ALD is that it allows the possibility to deposit thin alternate layers of different high-k materials (nanolaminates). This can be useful to tailor the dielectric properties of the stack, reduce leakage currents in the presence of possible crystallization processes or improve the interface in contact with the semiconductor [10,11].

In recent years, a lot of work has been devoted to physical and electrical characterization, as well as to reliability issues, of high-k dielectrics [12,13]. However, much less is known about their behavior in radiation environments. The study of ionizing radiation effects on high-k dielectrics is of special interest for space applications, but also for high energy physics experiments and to gain insight into possible effects of advanced micro/nanofabrication processes like e-beam or X-rays lithography.

Since the early days of microelectronics, radiation-induced effects on conventional SiO_2 dielectrics for CMOS technologies have been investigated [14–16]. Fortunately, the continuous miniaturization process has led to radiation-harder SiO_2 layers, with

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reduced charge trapping and thickness below the trapped-hole tunneling limit (around 3 nm) [15]. However, the introduction of new high-k dielectric materials brings some uncertainty in terms of their radiation hardness [16]. Different works have been published on radiation effects on a limited number of high-k dielectrics, being these mostly limited to irradiations with heavy ions or X-rays [17–20]. As a difference to irradiation with other particles like neutrons, protons or heavy ions, in the case of electron irradiation, the ionization damage is dominant against the displacement damage and this make them appropriate to evaluate ionizing radiation effects in dielectric materials. On the other hand, electrons are present in hostile radiation environments like advanced micro/nanofabrication processes, high energy physics experiments or the earth's natural radiation environment. For the case of the electrons trapped by the earth's magnetic field, typical energies of a few MeV are encountered, affecting the operation of electronic devices in artificial satellites [21].

In a previous work [22], we studied the effects of 2 MeV electron irradiation on the capacitance–voltage (C–V) and current–voltage (I–V) electrical characteristics of MOS capacitors with ALD-deposited layers of Al_2O_3, HfO_2 and nanolaminate dielectrics. The results showed similar radiation-induced charge trapping and interface states generation for the three high-k dielectrics, with an increase of the leakage current with electron irradiation fluence and no apparent impact of electron irradiation on dielectric breakdown voltage.

Few works in the literature have addressed the electrical stress effects on irradiated CMOS gate dielectrics, most of them dealing with conventional SiO_2-based dielectrics, where no much effects of the radiation-induced damage on the subsequent generation rate of traps during high-field stress was encountered [23–25]. More recently, some first attempts to evaluate possible combined effects between irradiation and electrical stress have been also carried out for HfO_2-based dielectrics [26,27].

The aim of the present work is to evaluate any possible interaction between the radiation-induced damage and the subsequent electrical stress degradation, focusing on the study of effective trapped charges, generation of interface states and presence of hysteresis.

2. Experimental

2.1. Sample description

Three high-k dielectric layers, Al_2O_3, HfO_2 and a 5-layer stack nanolaminate of them ($Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$), with physical thickness 11.6 nm, 10.5 nm and 10 nm, respectively, are studied. The layers were deposited by ALD in a Cambridge NanoTech Savannah 200 system. Al-gate MOS capacitors were fabricated on n-type and p-type silicon wafers. Three types of silicon substrates were used: n-type (phosphorus-doped with a resistivity 1–12 Ω cm), and two p-type substrates with different doping concentrations of boron, giving resistivity ranges of 4–40 Ω cm and 0.1–1.4 Ω cm, which are referred here as p-type 10 Ω cm and p-type 1 Ω cm, respectively. Although only results for a single p-type substrate may be given in the following discussions, the results were qualitatively and quantitatively similar for both p-type substrates. The used MOS capacitors are square-shaped with 6.4×10^{-5} cm^2 area (A). The obtained equivalent oxide thickness (EOT) values on the different silicon substrates ranged between 5.9 nm and 6.9 nm, 3.2 nm and 3.5 nm, and 4.3 nm and 5.1 nm for the Al_2O_3, HfO_2 and nanolaminate layers, respectively. Following this, the corresponding effective permittivity values ranged between 6.5 and 7.7, 11.8 and 13.1, and 8.2 and 9.7, respectively. A detailed description of the fabrication process can be found in [28].

2.2. Irradiation, electrical stress and electrical characterization

MOS capacitors were subjected to unbiased 2 MeV electron irradiations (the gates of capacitors were left floating) at room temperature for three different fluences ($\varphi = 1 \times 10^{14}$ e/cm^2, 1×10^{15} e/cm^2 and 1×10^{16} e/cm^2, with total ionizing doses about 2.5 Mrad(Si), 25 Mrad(Si) and 250 Mrad(Si), respectively), using the electron accelerator at Takasaki-JAEA in Japan.

In order to subject non-irradiated and 2 MeV electron-irradiated high-k dielectric MOS capacitors to electrical stress, an exponentially increasing stress current was forced to flow through the different dielectric layers, recording the evolution of gate voltage versus stress time until dielectric breakdown occurred, which was detected as a sudden drop of the measured gate voltage. Such a time dependent dielectric breakdown experiment will provide a reliability assessment of the different irradiated and non-irradiated layers for a potentially wide range of injected charge densities [29]. Fig. 1 shows a sketch of the experimental method used for the electrical stress. The specific values corresponding to the current densities and injection times used for each step are given in Table 1. The stresses were always performed in accumulation regime, i.e., corresponding to negative gate voltages with respect to the p-type substrates and positive gate voltages in the case of the n-type silicon ones. The injected charge density (Q_{inj}) is the sum of the injected charge densities corresponding to the different injection steps (Q_i).

C–V characteristics and electrical stresses were measured using an HP-4192 A LF impedance analyzer and an HP 4155B semiconductor parameter analyzer, respectively. C–V measurements were performed before and after each electrical stress step at a signal frequency (f) of 30 kHz for both, inversion to accumulation and accumulation to inversion voltage sweeps. The hysteresis was defined as the difference between the extracted flat-band voltages (V_{fb}) corresponding to the two voltage sweeps (hysteresis = $V_{fb\_inv\_to\_acc} - V_{fb\_acc\_to\_inv}$) [30]. An estimation of the effective trapped charge density (N_{eff_CV}), defined as a charge located at the insulator/silicon interface, was obtained from the comparison of the extracted V_{fb} values with the ones expected for an ideal MOS structure with 4.25 eV metal work function, corresponding to the aluminum gate electrode.

The conductance versus voltage (G–V) characteristics were also recorded. An estimation of the interface states density (D_{it}) was obtained from the peak of the parallel conductance (G_p) derived from the G–V measurements [31–33]:

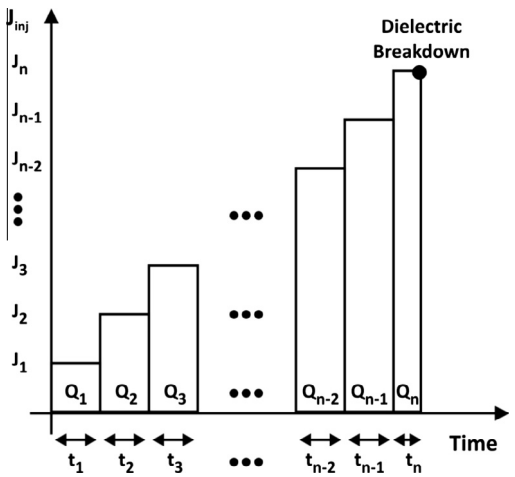

Fig. 1. Sketch of the exponential stress current experiment used for the electrical stress of the non-irradiated and 2 MeV electron-irradiated high-k dielectric MOS capacitors under study.