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An embedded nonvolatile memory cell with spacer floating gate for power management integrated circuit applications

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ABSTRACT

This paper describes a simple nonvolatile memory cell with a poly-Si spacer floating gate for power management integrated circuit applications. The proposed memory cell is fabricated using a 0.35 μm double-poly high-voltage CMOS process which includes PIP capacitor, LV (5 V), and HV (20 V) CMOS devices. The floating gates of the proposed cell are buried under a LDD spacer oxide; thus the unit cell can be scaled easily in the channel length direction. In addition, any extra photo masking step is not required for the proposed cell in the applied fabrication process. The proposed cell shows an acceptable threshold voltage window of up to 10^4 cycles and less than 2% threshold voltage shifts in an 85 °C retention test.

1. Introduction

Recently, embedded nonvolatile memory (NVM) cells for a power management integrated circuit (PMIC) have been reported by many semiconductor foundry companies [1–5]. These companies have made a considerable effort to integrate proper NVM cell structures into their own base-line high-voltage process technology.

For low-density applications of NVM, single poly-Si NVM cells consisting of two or more transistors are considered [2,4,5]. The single poly-Si NVM cell is an attractive solution for low density applications because it does not need extra photo steps. However, the single poly-Si NVM cell has a density limit because it requires an excessive unit cell size. On the other hand, stacked-gate NVM cells or silicon–oxide–nitride–oxide–silicon (SONOS) cells are usually considered for high-density applications because of the smaller unit cell size [1,3]. Unfortunately, these cells require additional photo masks or extra processing steps. Such additional photo masks and processing steps can create process complexity. As process complexity increases, the manufacturing cost may become expensive and production yield can be degraded.

An alternative method is an embedded NVM cell with a top-floating-gate (TFG) structure, as previously demonstrated by the authors of this study [6]. Even though the embedded TFG cell has a stacked-gate structure, it needs no additional photo masking step. However, the embedded TFG cell has inherent disadvantages that originated from the cell structure. First, the CG of the embedded TFG cell is placed under the floating gate (FG), thus the FG acts as a blocking layer during the salicide formation processing step. Therefore, the embedded TFG cell has greater parasitic resistance of the control gate (CG) word line. Second, the embedded TFG cell has a longer cell dimension in the channel length direction because the FG extension length over the CG will be long enough, considering FG-to-CG photolithography misalignment. As a result, shrinkage of the embedded TFG cell along a channel length direction is not easy.

In this paper, we present a newly developed scalable and cost-effective split-gate NVM cell for PMIC applications. The FG of the proposed cell is a poly-Si spacer which is buried under a lightly doped drain (LDD) spacer oxide; thus the channel length of the proposed cell can be comparable in size to a single MOSFET. For fabrication of the cell, a 0.35 μm high-voltage (HV) PMIC process with low-voltage (LV) CMOS, HV CMOS, and poly-insulator-poly (PIP) capacitor are applied. No extra photo masking step is required for the proposed cell fabrication.

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2. Memory cell structure and fabrication

2.1. Cell structure

The structure of the proposed cell is depicted in Fig. 1a. The gate of the proposed cell is composed of three parts. One gate at the center acts as the CG. Two gates at each side act as the FGs and these are connected electrically. As seen in Fig. 1a, the proposed cell is a split-gate type so it is free from over-erasure issues such as the embedded TFG cell in [6]. The proposed cell has further advantages. First, the two FGs of the proposed cell are formed by a spacer etch, thus the top sides of the CG can be exposed effectively. Therefore, the $TiSi_2$ layer is formed on top of the CG, the source, and the drain regions. As a result, parasitic resistances of the CG can be reduced for the proposed cell. Second, two FGs are buried under the LDD spacer oxide as shown in Fig. 1a. As a result, the channel length of the proposed cell can be comparable in size to a single MOSFET (metal–oxide–semiconductor field-effect transistor). In other words, the spacer-etched FGs cannot increase cell dimension along the channel length direction. Note that the embedded TFG memory cell has a larger unit cell dimension along the channel length direction because the bottom CG layer is enclosed with a top FG layer [6]. Third, the height of the proposed cell is scaled because the FGs are formed on the side of the CG. A reduction of cell height can enhance the uniformity of the chemical–mechanical-polishing (CMP) process for planarization of a poly-to-metal dielectric (PMD) layer. The TEM micrograph of the fabricated cell is shown in Fig. 1b. The thicknesses of the cell tunnel oxide and CG oxide are 12.5 and 50 nm, respectively. The proposed cell has a lightly doped drain (LDD) junction structure that is identical to 5 V low-voltage n-channel devices in the applied fabrication process flow.

Fig. 1c shows the top view of the proposed cell, whereby conventional NOR array configuration can be applied for the proposed cell. Similar to a typical NOR array, a metal-1 layer is used for the bit lines. For cell isolation, each cell has an isolated CG pattern and an FG spacer surrounding the isolated CG pattern. The individual CG patterns are connected with a metal-2 layer used for the word lines. The dimensions of the proposed cell along the channel width and length direction are 4.0 and 8.5 F, respectively. Detail design rules are annotated in Fig. 1c.

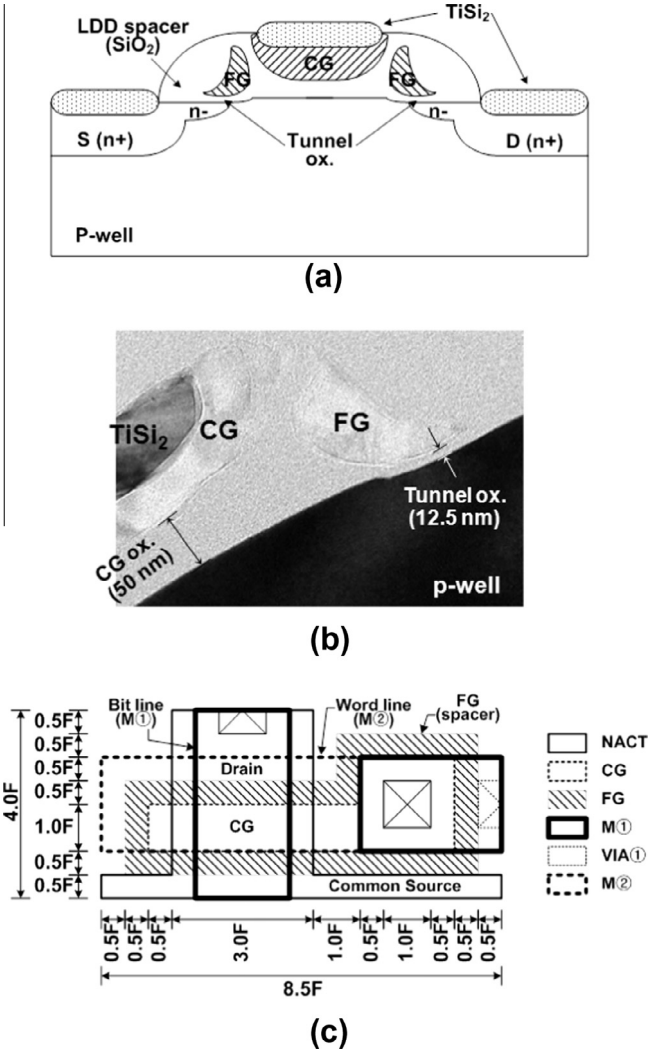

Fig. 1. Structure of the proposed cell; (a) cross section, (b) TEM micrograph of the fabricated cell, and (c) top view.

2.2. Fabrication

The major process flow is shown in Fig. 2. The proposed cell is fabricated using a 0.35 μm double-poly and double-metal HV process. The LV and HV CMOS devices (5 and 20 V), and PIP capacitor are available in that process. The bottom and top poly-Si layers in the PIP capacitor are applied for the CG and FG in the proposed NVM cell. The tunnel oxide under the FG is identical to the gate oxide of the LV CMOS devices and the thicker gate oxide under the CG is identical to the gate oxide of the HV CMOS devices. Therefore, an extra photo masking step is not necessary for fabrication of the proposed cell.

The brief process flow is as follows: high-voltage n- and p-well formation, n- and p-drift junction formation, local oxidation of silicon (LOCOS) isolation, CG gate oxidation (50 nm), undoped poly-Si deposition for CG, CG doping by ion implantation (Ph+, 30 keV, $5.1 \times 10^{15}/cm^2$), SiO_2/Si_3N_4 deposition (Ox./Nit. = 7/40 nm), Si_3N_4 anneal (steam anneal, T_{OX} = 140 nm on monitor wafer), CG define, thermal oxidation (50 nm), oxide wet etch, LV gate oxidation (tunnel oxide, 12.5 nm), FG poly-Si deposition (doped poly-Si, 250 nm), FG etch, reoxidation, n-LDD junction formation, LDD oxide deposition (250 nm), LDD spacer formation, n + junction formation, $TiSi_2$ formation, contact, and metallization.

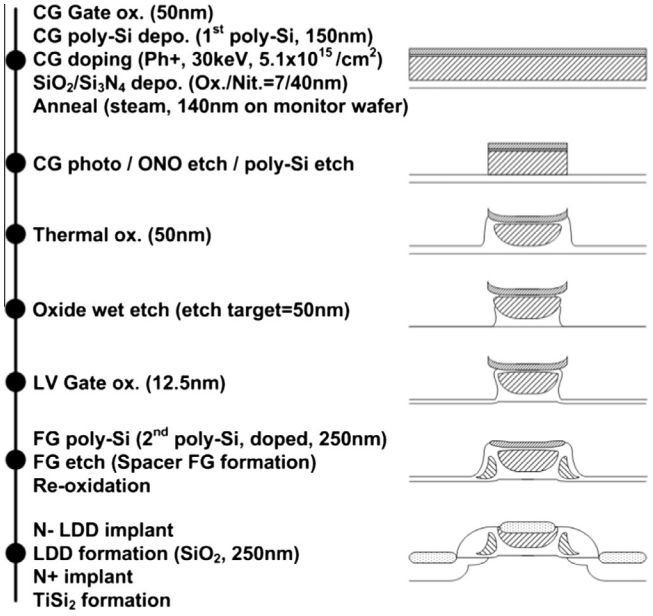

Fig. 2. Cross sectional view of major process sequence of the proposed cell.