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Improvement of metal gate/high-*k* dielectric CMOSFETs characteristics by neutral beam etching of metal gate

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ABSTRACT

For the metal gate patterning of metal gate/high-*k* dielectric complementary metal–oxide–semiconductor field effect transistors (CMOSFETs), plasma induced damage (PID) was identified during the etching by a conventional reactive ion etching (RIE) and, a neutral beam etching (NBE) technique. NBE uses reactive radical beam instead of reactive ions for RIE. Improved device characteristics such as the mobility, the transconductance, subthreshold slope, and drain current could be observed. Particularly, the application of the NBE to PMOSFET was more effective than that to NMOSFET. This improvement was related to the decreased interface trap density at the gate dielectric of CMOSFEETs.

1. Introduction

As the critical dimension (CD) of the metal–oxide–semiconductor field effect transistor (MOSFET) is scaled down to 45 nm node and below, high dielectric constant materials become an attractive alternative to SiO_2. However, the poly-Si with high-*k* dielectric shows a limitation in the work function tunability at the poly-Si/M_eO_x interfaces. This limits the threshold voltage control in complementary MOSFETs (CMOSFETs), particularly in *p*-channel MOSFET (PMOSFET). Therefore, a metal gate with high-*k* dielectric has been considered [1].

For the metal gate patterning, reactive ion etching (RIE) has been generally used to etch anisotropically for the accurate CD control. Previous works have shown that using HBr/Cl_2 gas, high TiN etch rate was obtained in addition to the highly anisotropic etch profile of poly-Si/TiN/HfO_2/Si in the inductively coupled plasmas (ICPs) [2], and CD was controlled not exceeding 2 nm and profiles close to vertical were achieved in sub-45 nm TaN/HfAlO/Si [3]. However, during these metal gate etching, plasma induced damage (PID) can be generated and it can degrade the electric characteristics of metal gate/high-*k* dielectric CMOSFETs [4,5].

PID during the etching of a gate structure by RIE consists of plasma induced charging damage (PICD) and plasma induced edge damage (PIED) [6]. PICD is mainly caused by the high-field stressing of thin gate oxides during plasma processing. A local imbalance of the ion current density from the plasma to the substrate or the differences in the etch endpoint during the gate etching induces plasma induced charging current (PICC) across the gate oxide. And, a high stress voltage developed by the PICC across the gate oxide results in forming interface traps near the gate oxide [7]. In the case of poly-Si/SiO_2/Si, PICD can be formed during the poly-Si etching. However, in another case of poly-Si/TiN/HfO_2/Si, it can be formed during the metal gate etching because the presence of a metal gate can prevent local imbalanced ions during poly-Si etching. It is known that, in poly-Si/aggressively scaled SiO_2 CMOSFETs, PICD is no longer a problem because of the low stress voltage for a given PICC [8]. However, given the higher physical thickness of high-*k* dielectrics compared to SiO_2, the problem could be reintroduced due to higher stress voltage. [9,10].

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Neutral beam etching (NBE) has been previously introduced by many researchers to remove possible PID during the etching of semiconductor devices. The reactive radical beam was generally formed by neutralizing the reactive ions using various methods such as neutralization by the reflection of ions on the low angle reflector, neutralizing reflection on the sidewall of the grid hole during the extraction of ions from a plasma source, etc. [11–15]. Previously, using CHARM® 2 monitoring wafers after NBE no significant change in positive charging, negative charging and UV damage was observed compared to RIE. NBE has been applied to a MOS capacitor structure for the possibility of removal of PICD [11] and also other applications such as the barrier layer etching in anodic aluminum oxide (AAO) [12], GST etching in phase change memory (PCM), recently [13]. However, the effect of NBE on PICD in metal gate/high-*k* dielectric CMOSFETs has not been systematically studied.

In this article, a NBE has been applied to the etching of CMOSFET metal gate composed of poly-Si/TiN/HfO_2/SiO_2/Si after the poly-Si etching and the effect of the metal gate etching using NBE on the electrical characteristics of CMOSFETs was compared with those etched using conventional RIE.

2. Experimental

Metal gate/high-*k* dielectric CMOSFETs with the gate width (W) of 10 μm and the gate length (L) of 1 μm were fabricated using a standard complementary MOS process except for TiN metal gate etching. The gate stacks include 1000 Å poly-Si/100 Å TiN/30 Å HfO_2/interfacial 10 Å SiO_2 on Si substrate. TiN metal gate was etched by an optimized RIE or NBE process. RIE was carried out using rf-biased Cl_2-based inductively coupled plasma (ICP). The NBE was carried out for 2 min 30 s using a low angle reflected HBr/Cl_2 NBE system composed of a three-grid ICP ion source installed with a low angle reflector in front of the ICP ion source for the neutralization of reactive ion beam (>90% neutralization efficiency). The details of the NBE system can be found [11]. After the metal gate etching with the RIE or the NBE, the high-*k* dielectric was removed with a HF-based wet etching after slight Ar^+ ion physical bombardment by a RIE system.

Equivalent oxide thickness (EOT) was extracted from the measured capacitance–voltage (C–V) curves on a MOS capacitor (MOSCAP) with an area of 200 μm^2 using North Carolina State University (NCSU) CVC model and the EOT was calculated to be about 1.2 nm for the etching of metal gate using both RIE and NBE indicating no variation of EOT after the metal gate etching. Transmission electron microscope (TEM) of the CMOSFET gate after the NBE of TiN gate metal is shown in Fig. 1. As shown in the figure, a similar slightly tapered etch profile could be obtained after the TiN metal gate etched by (a) RIE and (b) NBE.

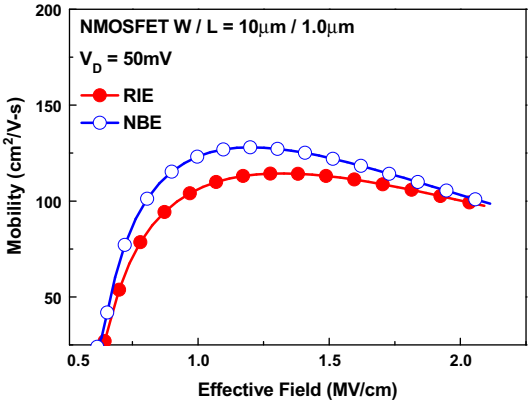

Fig. 2. Effective mobility for NMOSFET with W/L = 10 μm/1 μm after RIE and NBE.

3. Results and discussion

PICD affects the interface state in the gate oxide of the CMOSFET. The effective field electron mobility is known to be more sensitive to the interface state than other MOS parameters [16]. Fig. 2 shows the electron mobility measured as a function of effective field for the NMOSFETs with W/L = 10 μm/1 μm after RIE and NBE. The mobility was extracted using NCSU mob2d model [17]. As shown in the figure, the maximum effective field electron mobility for NBE (127.2 cm^2/V s) was 10.1% higher than that for RIE (114.4 cm^2/V s). This is attributed to the low PICD inducing interface states at the gate oxide. Note that the effective field electron mobility of the NMOSFET after RIE is consistent with the previous report [1].

MOS parameters (transconductance (G_m), threshold voltage (V_{th}), subthreshold swing (SS), drain current (I_D) and gate leakage current (I_G)) are also sensitive to PICD. This PICD has the polarity depending on a gate dielectric. In the case of SiO_2, PICD has the different polarity, which leads to shift V_T of PMOSFET in the opposite direction to NMOSFET. However, in another case of a high-*k* dielectric (HfO_2), V_T is moved to the same direction, positively in both NMOSFET and PMOSFET [18]. The typical method of PICD estimation is to detect the degradation of the MOS parameters directly. Therefore, MOS parameters were extracted from the I_D–V_G mea-

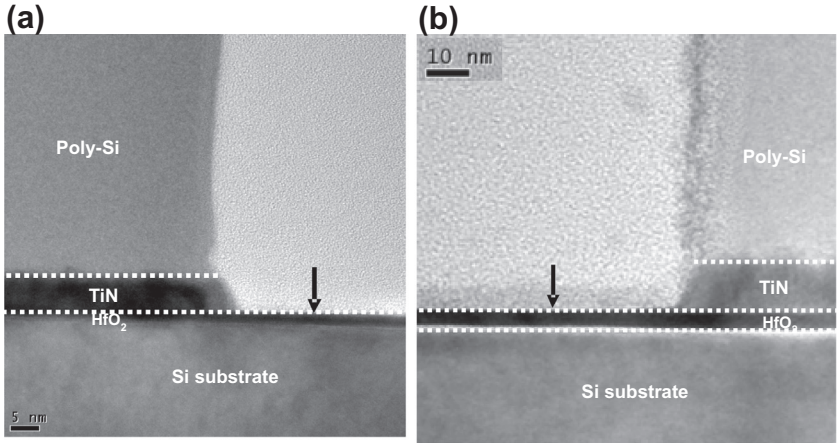

Fig. 1. Cross-sectional TEM images of the gate stacks after (a) RIE and (b) NBE.