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Compensation of oxygen defects in La-silicate gate dielectrics for improving effective mobility in high-k/metal gate MOSFET using oxygen annealing process

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ABSTRACT

Oxygen incorporation for compensation of oxygen defects is investigated with La-silicate dielectrics in directly contacted with the Si substrate. The amount of oxygen is controlled by the temperature of annealing in oxygen atmosphere (oxygen annealing) and the thickness of the gate electrode. The positive shift in flatband voltage (V_{FB}) by oxygen incorporation is an experimental evidence for defects compensation in La-silicate dielectrics. Optimum oxygen annealing provides the V_{FB} shift toward positive direction without increasing equivalent oxide thickness (EOT). Although the oxygen annealing degrades the interfacial property at La-silicate/Si interface, subsequent forming gas annealing (FGA) can recover the interfacial property. It is experimentally revealed that the positive V_{FB} shift of La-silicate dielectrics is stable even after subsequent FGA. The supplied oxygen in La-silicate is expected to maintain even after reducing process. Movement of Fermi level toward the Si valence band edge caused by oxygen incorporation is successfully observed by XPS. Moreover, no chemical reaction between La-silicate and Si substrate by oxygen annealing are confirmed from TEM observation and analyses of X-ray photoelectron spectra. It is experimentally demonstrated that effective hole mobility can be improved without increase in EOT by combination of oxygen annealing and FGA.

1. Introduction

High-k/metal gate stacks has been introduced in metal oxide semiconductor field effect transistors (MOSFET) to replace the conventional SiO_2/poly-Si gate stacks for scaling in an equivalent oxide thickness (EOT) [1,2]. The scaling in EOT with high-k/metal gate stacks is also important to suppress the short-channel effect and threshold voltage variability in highly scaled MOSFETs [3,4]. However, a thin layer of SiO_2 is typically formed as interfacial layer to suppress the increase in interface state density or inversion carrier mobility degradation [5]. EOT below 0.5 nm is limited by the presence of SiO_2 interfacial layer. Thus, a structure directly in contacted with silicon (Si) is strongly required for further EOT scaling with high-k/metal gate stacks. Recent reports have been demonstrated that EOT below 0.5 nm can be attained with a direct contact high-k/Si structure using Hf-based oxides to inhibit or scavenge the SiO_2 interfacial layer by careful process techniques [6,7]. Besides, it has been reported that the direct contact high-k/Si structure can be also easily achieved with La_2O_3 for gate dielectrics due to a formation of La-silicate layer as the compositional transition layer at the La_2O_3/Si interfaces and fairly nice nMOSFET operation has been observed with scaled EOT [8].

One of the essential issues for high-k/metal gate stacks is how to compensate oxygen vacancies in high-k dielectrics associated with its ionic nature [9]. The oxygen vacancies strongly affect on the electrical characteristics of MOSFETs [10–12]. Therefore, careful device process to compensate the oxygen deficiency in the high-k without any increase in EOT should be conducted. One of the effective ways to compensate the oxygen defects is to incorporate oxygen into high-k dielectrics. Since oxygen vacancies are positively charged, flatband voltage (V_{FB}) or threshold voltage (V_{th}) shift to positive direction by oxygen incorporation is an experimental evidence for defects compensation. Actually, V_{FB} shift by 500 mV toward Si valence band edge has been reported by oxygen incorporation into HfO_2 through thin TiN gate electrode without increase in EOT [13]. Thus, it is of great interest to conduct the oxygen incorporation for improving MOSFET characteristics without penalty in EOT.

The objective in this study is to investigate the effect of oxygen incorporation into La-silicate dielectrics through the metal gate electrode. Since La_2O_3 absorbs moisture to form hydroxides, $La(OH)_3$, by air exposure, *in situ* deposition of metal after La_2O_3 deposition is introduced to avoid formation of $La(OH)_3$ [14]. Therefore, the method for

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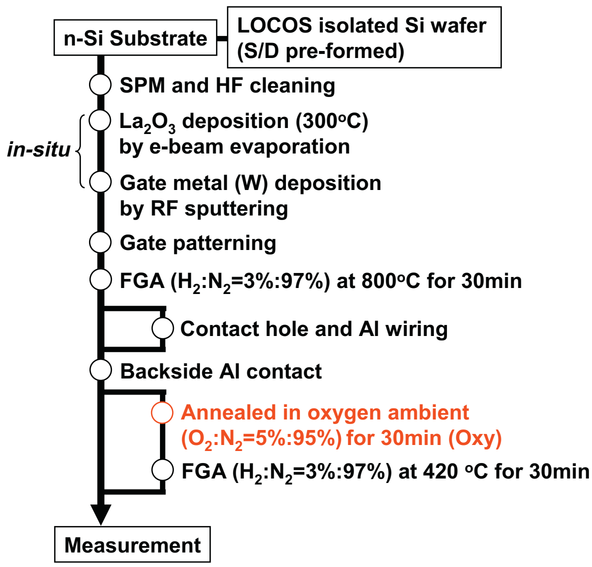

Fig. 1. Process flow of MOS capacitors and MOSFETs using gate last process.

supplying oxygen through gate electrode is attracted much attention [13]. Optimum device process conditions including the annealing temperature and a thickness of gate electrode is examined by electrical and physical characterizations. The impact of the process is also discussed through fabrication and characterization of pMOSFETs.

2. Device fabrication and experiment

La_2O_3 was deposited on HF-last n-Si wafer for MOS capacitors by e-beam evaporation in an ultra-high vacuum chamber, followed by *in situ* W (tungsten) metal deposition by RF sputtering. The metal was patterned by reactive ion etching (RIE) with SF_6 chemistry to form gate electrodes. The substrate impurity concentration of MOS capacitors is 3×10^{15} cm^{-3}. The samples were post-metallization annealed in forming gas ambient (H_2:N_2 = 3%:97%) at 800 °C for 30 min to form the La-silicate by the reaction with Si substrate [8]. Source and Drain pre-formed n-Si (100) substrates were also utilized to fabricate pMOSFETs. The substrate impurity concentration of MOSFETs is 3×10^{16} cm^{-3}. Al was deposited on the source/drain region and back side of the substrate as a contact. Annealing in oxygen ambient (oxygen annealing) for 30 min (Oxy) was applied to supply additional oxygen into La-silicate. Diluted oxygen (O_2:N_2 = 5%:95%) was used for oxygen annealing. Finally, recovery annealing (FGA) was performed. Process flow is summarized in Fig. 1. EOT and V_{FB} were estimated by NCSU CVC program [15]. Split-CV method was employed to measure an effective mobility of pMOSFETs [16].

3. Results and discussion

3.1. Electrical characteristics of MOS capacitors

Fig. 2a shows the effect of oxygen annealing on C–V characteristics with La-silicate dielectrics. Physical thickness of *W* metal is confirmed to be 5 nm from cross sectional TEM image. The *C–V* curves shifted to the positive direction with the increase in the oxygen annealing temperature. This experimental result suggests that the additional oxygen can be successfully introduced into the La-silicate dielectrics during the oxygen annealing. To further understand the influence of the oxygen annealing, V_{FB} shift and EOT increase are plotted as a function of the oxygen annealing temperature in Fig. 2b. Although V_{FB} shift monotonically increases with the increase in annealing temperature below 350 °C, the V_{FB} shift starts to saturate above 360 °C. Moreover, increase in EOT is observed at a temperature above 350 °C. It indicates that excess oxygen incorporation induce the interfacial layer growth [17]. However, large positive V_{FB} shift without EOT increase can be attained at a temperature of 340 °C.

The *C–V* curves of MOS capacitors turn up in inversion region shown in Fig. 2a. It implies de-passivation of dangling bonds or newly created minority carrier generation center after oxygen annealing [18]. It is well known that interface property strongly affects the inversion carrier mobility of MOSFET. The FGA is effective to terminate the dangling bonds at SiO_2/Si interface [19]. Thus, the FGA at 420 °C for 30 min was performed after oxygen annealing. Fig. 3a shows the effect of subsequent FGA on *C–V* characteristics with La-silicate. The subsequent FGA showed improvement in the *C–V* characteristics while maintaining the V_{FB} at positive value even with the annealing in reducing ambient. Fig. 3b shows the comparison of interface state density (D_{it}) as a function of annealing conditions measured by conductance method [20]. The interface state density is increased after oxygen annealing while subsequent FGA can completely recover the interface state density. These results suggest that the supplied oxygen in La-silicate is maintained and interface state density can be successfully passivated by subsequent FGA. These are interesting and important experimental results. Although the V_{FB} behavior of HfO_2 dielectrics is reported to be unstable and the negative V_{FB} shift occurs after FGA at temperature below 400 °C [18], our results are completely different and suggest that MOSFET characteristics may be improved by subsequent FGA.

Next, effect of *W* metal thickness on V_{FB} shift was examined. Fig. 4 shows the positive V_{FB} shift as a function of *W* thickness.

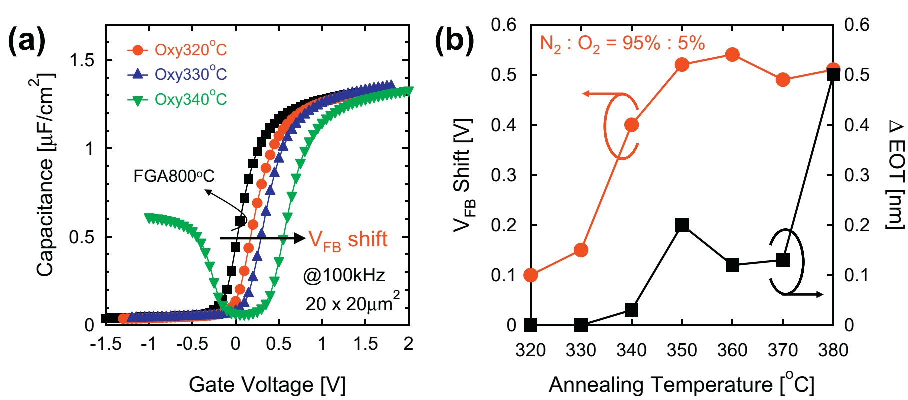

Fig. 2. (a) Effect of oxygen ambient annealing on *C–V* characteristics with La-silicate dielectrics. (b) V_{FB} shift and EOT increase with increase in oxygen annealing temperature.