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Solution processed inverter based on zinc oxide nanoparticle thin-film transistors with poly(4-vinylphenol) gate dielectric

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ABSTRACT

An enhancement-load inverter using bottom-gated ZnO nanoparticle thin-film transistors and a polymer gate dielectric is demonstrated. The deposition of the ZnO active layer is done by spin coating of a colloidal dispersion and is hence cost-effective. Since the maximum process temperature is 200 °C, the presented device is furthermore suitable for plastic substrates. Although hysteresis is observed, the inverter shows reasonable transfer characteristics with a gain of up to 5.5 V/V at a supply voltage between 10 V and 15 V, whereas the static power dissipation is lower than 6 μW.

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1. Introduction

During the last years, inorganic semiconductors have received much attention for low-cost electronic applications [1,2]. In particular, zinc oxide (ZnO) is a promising candidate for flexible, transparent and printable thin-film transistors (TFT). With regard to printability, ZnO is commonly deposited as nano-structured material forms like nanorods, nanowires and nanoparticles [2,3] or by sol–gel method [4], whereas either the nanomaterial or the precursors are spin-coated on the surface. Even TFTs integrated by inkjet-printing technique have been demonstrated [5]. However, solution-processing via the sol–gel route is in need of relatively high temperatures for the precursor decomposition [6,7]. Though showing reasonable performance, the reports of nanomaterial-based devices are limited to individual TFTs, and a post-treatment of the active layer (high-temperature annealing or laser sintering) is often needed in order to improve the conductivity of the semiconductor film [8–10]. Logic circuits (i.e. inverters) are usually integrated by sputtering or atomic layer deposition of ZnO or related materials [11–13]. Therefore, inverter circuits based on enhancement-type, bottom-gated Schottky-barrier Drain/Source TFT and using ZnO nanoparticles as active layer material are presented in this paper. All processes are kept as simple and cost-effective as possible: ZnO is deposited by spin-coating of a commercial, chemically non-modified colloidal suspension and poly(4-vinylphenol) (PVP) is used as gate dielectric [14]. Furthermore, the maximum temperature during the integration flow is $\leqslant$200 °C to demonstrate a process, which is compatible to plastic substrates.

Although the noise margins are still asymmetric and the switching behavior suffers from hysteresis, the presented inverters show very reasonable characteristics with a gain of up to 5.5 V/V and a power dissipation less than $P = 5.5$ μW.

2. Device integration and structure

The inverter devices were integrated on lightly boron-doped 4-inch silicon wafers, which were thermally oxidized for electrical insulation. The gate electrodes were deposited by e-beam evaporation of aluminum (50 nm) and structured by wet-etching.

A thin-film of PVP ($M_w \approx 25{,}000$, Sigma-Aldrich) was then spin coated atop the gate electrodes from a 0.08 wt% PVP-solution in 2-methoxy-1-methylethylacetate (PGMEA) with 1.7 wt% of the cross-linking agent poly(melamine-co-formaldehyde)-methylated (PMCF-m, $M_w \approx 432$, Sigma-Aldrich). The PVP-solution (2 ml) was dispensed at a low spin speed of 800 rpm followed by a high-speed spin at 3000 rpm for 30 s. After the coating, the samples were immediately pre-baked at 100 °C for 60 s to ensure removal of

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the PGMEA, and then cured at 200 °C for 30 min to activate the cross-linking reaction. Due to simplicity reasons, the cross-linking bake was performed in ambient atmosphere at normal pressure without a substantial loss of electrical quality. A PVP layer thickness of 180 nm was measured by surface profiling. Contact vias for access to the gate electrodes were opened in the PVP using RIE with an O_2-plasma (gas flow: 10 sccm, pressure: 100 mTorr, process time: 135 s) at a rf power density of 0.3 W/cm^2. The etch selectivity to the photoresist (Clariant AZ 5214E) is higher than 4 and hence sufficient for structuring the PVP layer. After stripping the resist in acetone, the PVP layer remains unaffected.

The ZnO nanoparticles were deposited from an aqueous suspension by spin-coating as well. The dispersion (23.3 wt%) of zinc oxide nanoparticles (*AdNano ZnO 20 DW*) was received from EVONIK DEGUSSA GMBH. The primary particles adhere to each other forming strong agglomerates, which cannot be separated. Therefore, the effective particle size is in the range of 100 nm [15]. The spin-coating was performed with a low-speed spinning at 800 rpm for dispensing the dispersion and a high-speed spinning at 1000 rpm for 30 s. Subsequently, the sample was baked on a hot-plate at 110 °C for 5 min leading to a transparent ZnO film. SEM analysis of the layer cross section and the AFM topography with a height variation of approximately ±25 nm (Fig. 1a) revealed a layer thickness of 300–350 nm, while the root mean square roughness is 9.2 nm. To ensure sufficient adhesion and mechanical stability of the particle film, the samples were annealed at 200 °C for 1 h in ambient air again. As can be seen from the SEM micrograph and the AFM topography of the ZnO nanoparticle film in Fig. 1, the deposition and annealing processes led to an appropriate layer which exhibited suspension-typical small agglomerates with diameters of less than 100nm as well as primary particles [15]. With regard to the effective particle size, the layer is relatively thin and some layer defects, i.e. pin-holes, can already be observed (marked by circles). The film quality could be enhanced either by

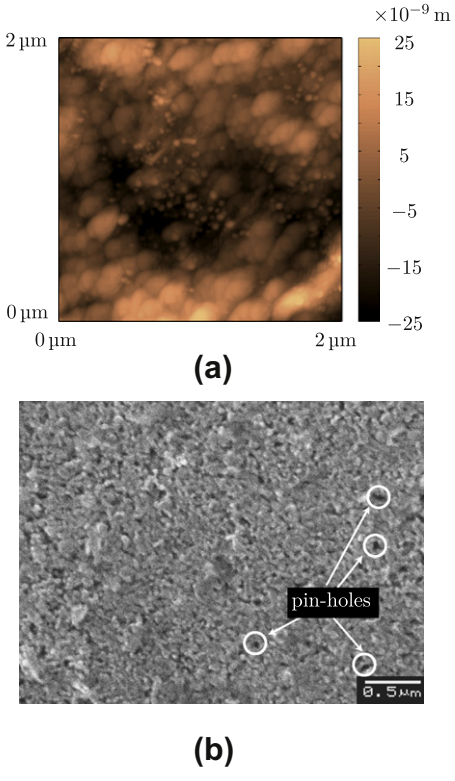

Fig. 1. AFM topography (a) and SEM micrograph (b) of ZnO nanoparticle layers.

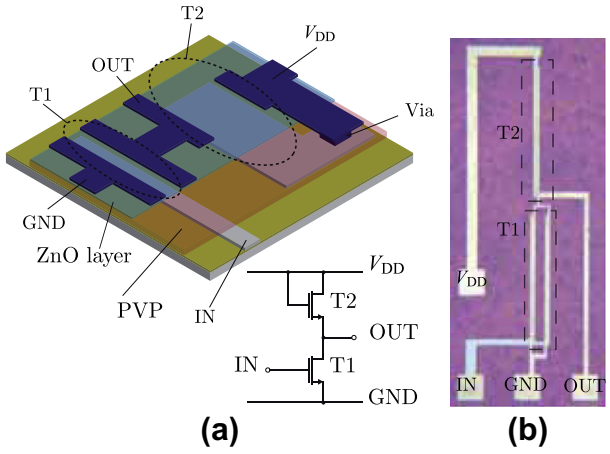

Fig. 2. 3D-graph, schematic (a) and optical micrograph (b) of the presented inverter circuit.

using an organic dispersion medium to improve the wetting of the substrate or by addition of appropriate surfactants to the nanoparticle suspension. Both possibilities would lead to organic residuals which may impair the electrical layer properties in turn and have to be burnt at a relatively high temperature.

At last, source and drain electrodes were structured by a gentle lift-off technique in n-methyl-2-pyrrolidone (NMP) after e-beam evaporation of aluminum (200 nm). Fig. 2a shows the 3D-graph and the schematic of the integrated inverter circuit. An optical micrograph is presented in Fig. 2b.

3. Results and discussion

With the PVP layer thickness of 180 nm, capacitance characterization of the PVP using an AGILENT 4294A impedance analyzer yields a relative permittivity of $\epsilon_r = 5.9$ at 1 kHz. The relative dielectric constant decreases from 6.1 to 4.8 in the frequency range from 50 Hz to 1 MHz, which is still sufficient for medium frequency applications like RFID. Electrical characterization of the TFTs and the inverters was performed using a HP 4156A parameter analyzer under ambient conditions in darkness at a relative humidity of *RH* = 33%.

3.1. Individual transistors

The transfer and output characteristics of a typical individual transistor with a channel length $L = 1.5$ µm and a width $W = 500$ µm are shown in Fig. 3. As can be seen, the proposed integration route leads to n-type enhancement transistors operated under moderate voltage conditions. The devices exhibit a significant amount of hysteresis, which is probably due to mobile ions. The hysteresis is already well-known from PVP dielectrics in organic field-effect transistors as well as in inorganic nanoparticle devices [16,17]. The threshold voltages for forward and backward sweeps are $V_{th} = 1.4$ V and $V_{th} = 0.2$ V, respectively. Therefore, a hysteresis in the switching behavior of logic inverters is expected. Analysis of ten switching TFT showed a standard deviation of $\sigma_{V_t} = 2.26$ V and a mean value of $\overline{V}_t = 3.49$ V. The wide spread is presumably caused by varying contact properties and layer inhomogenities [18]. Since the threshold voltages are widely distributed, reproducibility will be a main issue for future experiments, but does not limit the demonstration and analysis of inverter devices in the actual state of research so far.

The field-effect mobility, extracted from the transfer characteristics, is $\mu_{FE} = 3.2 \times 10^{-3}$ cm^2 (V s)$^{-1}$ and therefore moderate com-

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